MB171 IDTV
SERVICE MANUAL

Table of Contents

IMPORTANT
Before removing the rear cover from the TV for servicing, make sure that no cables are fixated to the cover. Release the cables from their clamps and disconnect (if any). Failure to do so may damage the wires and/or other components of the TV.

1. INTRODUCTION

17MB171 main board is driven by MTK SOC. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU.

This board can drive 50Hz HD & FHD panels.

Key features include:

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- The ACE PRO Video Processor
- Home theatre sound processor
- Rich internet connectivity and completed digital home network solution
- Dual-stream decoder for 3D contents
- Multi-purpose CPU for OS and multimedia
- Security Engine and TEE
- Peripheral and power management
- Embedded DRAM (for connected option)

Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Back AV (CVBS, R/L_Audio)
- 1 PC input(Common)
- 3x HDMI inputs (with ARC option from 2nd or 3rd input)
- 1 Common interface(Common)
- 1 Optic/ Quax S/PDIF output
- 1 Headphone(Common)
- 2 USB(2X Side) and 1x internal USB for Wifi/Bluetooth
- 1 Ethernet-RJ45

2. T/T2/C/A TUNER (U118)

Description

The Si2151 is Silicon Labs' sixth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wirewound inductors or LNAs, the Si2151 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2151 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners. The Si2151 offers increased immunity to WiFi and LTE interference, eliminating the need for external filtering. For the best performance with next-generation digital TV standards, such as DVB-T2/C2, the Si2151 delivers industry-leading phase noise performance.

Features

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVBT2/T/C2/C, ISDB-T/C, DTMB
- 1.7 MHz, 6 MHz, 7 MHz, 8 MHz, and 10 MHz channel bandwidths
- 42-1002 MHz frequency range
- Industry-leading margin to A/74, NorDig, DTG, ARIB, EN55020, OpenCable™,DTMB
- Lowest BOM for a hybrid TV tuner
  - No balun, SAW filters, or external inductors required
  - Increased ESD protection on 4pins
- Best-in-class real-world reception
  - Lowest phase noise
  - High Wi-Fi and LTE immunity
- Low power consumption
  - 3.3 V and 1.8 V power supplies
  - Integrated 1.8 V LDO for 3.3 V singlesupply operation
- Integrated power-on reset circuit
- Standard CMOS process
- 3x3 mm, 24-pin QFN package

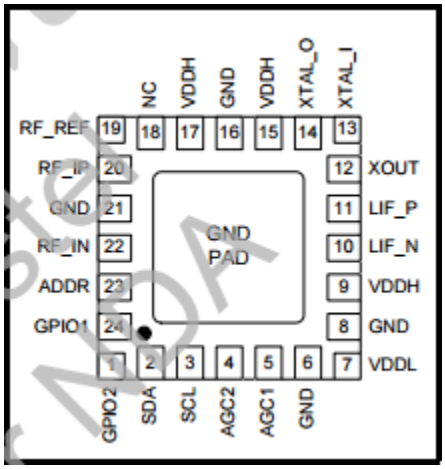


Figure 1: Si2151 Pin description

Pin Number(s)	Name	I/O	Description
1*	GPIO2	I/O	General purpose input/output #1
2	SDA	I/O	I^2C data input/output
3	SCL	I	I^2C clock input
4*	AGC2	I	LIF output amplitude control input #2
5*	AGC1	I	LIF output amplitude control input #1
6	GND	S	Ground
7	VDDL	S	Low supply voltage, 1.8 V (leave caps connected for single supply case)
8	GND	S	Ground
9	VDDH	S	High supply voltage, 3.3 V
10	LIF_N	O	Negative LIF differential output to SoC or DTV/ATV demodulator
11*	LIF_P	O	Positive LIF differential output to SoC or DTV/ATV demodulator
12	XOUT	O	Output reference clock to secondary tuner or receiver
13	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)
14	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)
15	VDDH	S	High supply voltage, 3.3 V
16	GND	S	Ground
17	VDDH	S	High supply voltage, 3.3 V
18*	NC	NC	No connect
19	RF_REF	O	RF reference voltage output
20	RF_IP	I	RF input (positive)
21	GND	S	Ground
22	RF_IN	I	RF input (negative)
23	ADDR	I	I^2C address select
24*	GPIO1	I/O	General purpose input/output #1

***Note:** Pin should be left floating if unused.

3. S/S2 TUNER (U3) OPTIONAL

Description

M88TS6011 is a single-chip, direct-conversion tuner for digital satellite receiver applications. It offers the industry's most integrated solution to a satellite tuner function, simplifying the front-end designs.

This device incorporates the following functional blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with an integrated auxiliary clock output.

As a result of integrating all these blocks, the M88TS6011 has the least number of pins compared with other conventional solutions, and requires the least external components. In typical applications, the M88TS6011 requires only one crystal, one matching network, and a few external capacitors. The device also has the industry's smallest latency, as it uses a fast locking PLL and a fast settling DC offset cancellation architecture.

The M88TS6011 can be configured via a 2-wire serial bus. The chip is available in a 16-pin QFN package.

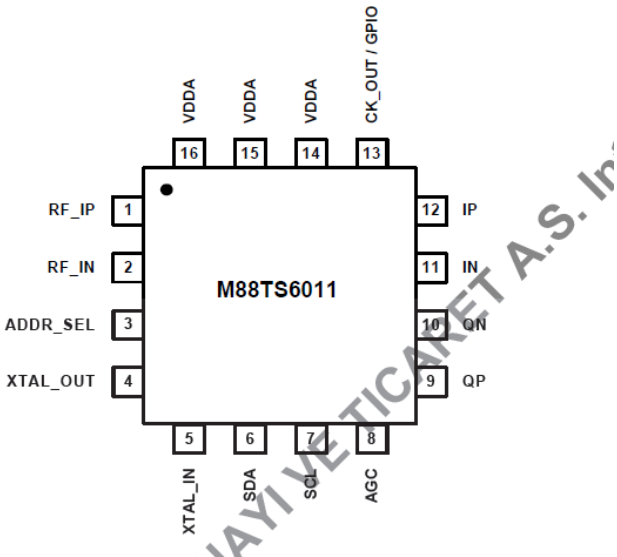
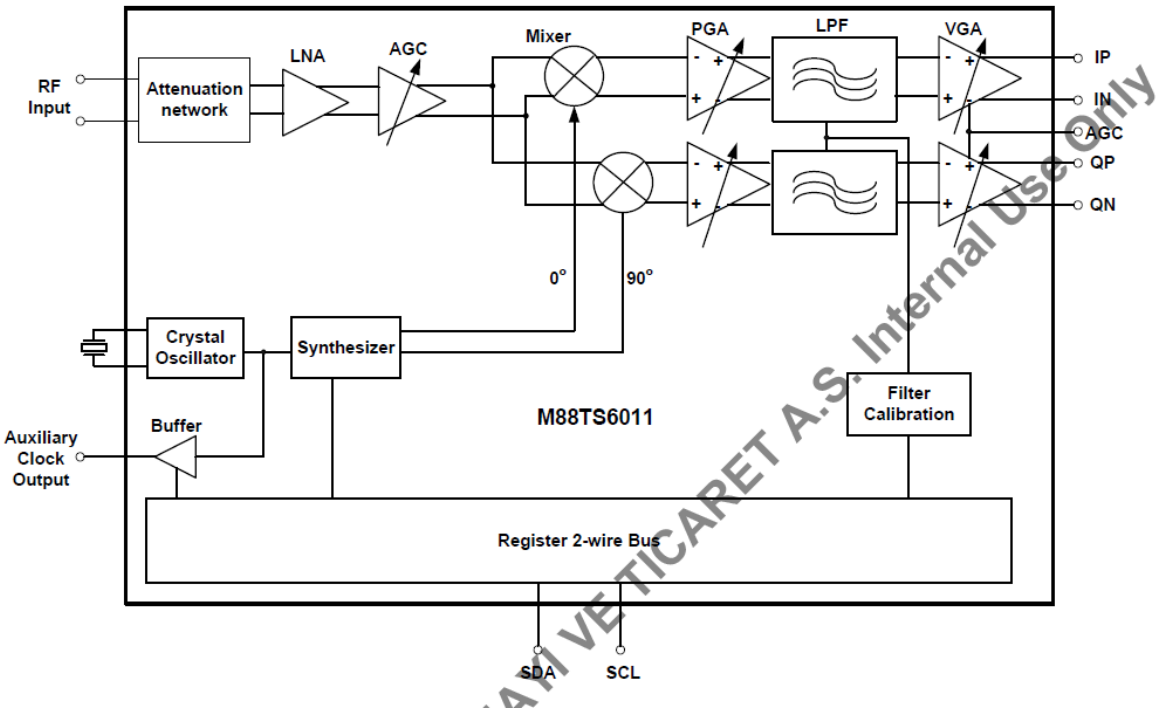


Figure 2: Pin description

Features

- Single-chip tuner
- Compliant with DVB-S/S2 and ABS-S standards
- Support QPSK, 8PSK, 16APSK and 32APSK
- Direct-conversion from L-band to baseband
- Symbol rate: 1 to 45 Msymbol/s
- Integrated VCOs and PLL, with on-chip inductors, varactors and loop filter
- Integrated baseband filters: 6 MHz to 40 MHz bandwidth
- Integrated RF AGC for optimal performance
- Integrated baseband DC offset cancellation removes external loop filters
- Excellent immunity to strong adjacent undesired channels
- Integrated clock driver provides auxiliary clock output for other devices
- Support sleep mode
- 2-wire serial bus with 3.3 V compatible logic levels
- Power supply: +3.3 V
- Package:16-pin E-PAD QFN
- RoHS compliant

Block Diagram



4. AUDIO AMPLIFIER STAGES

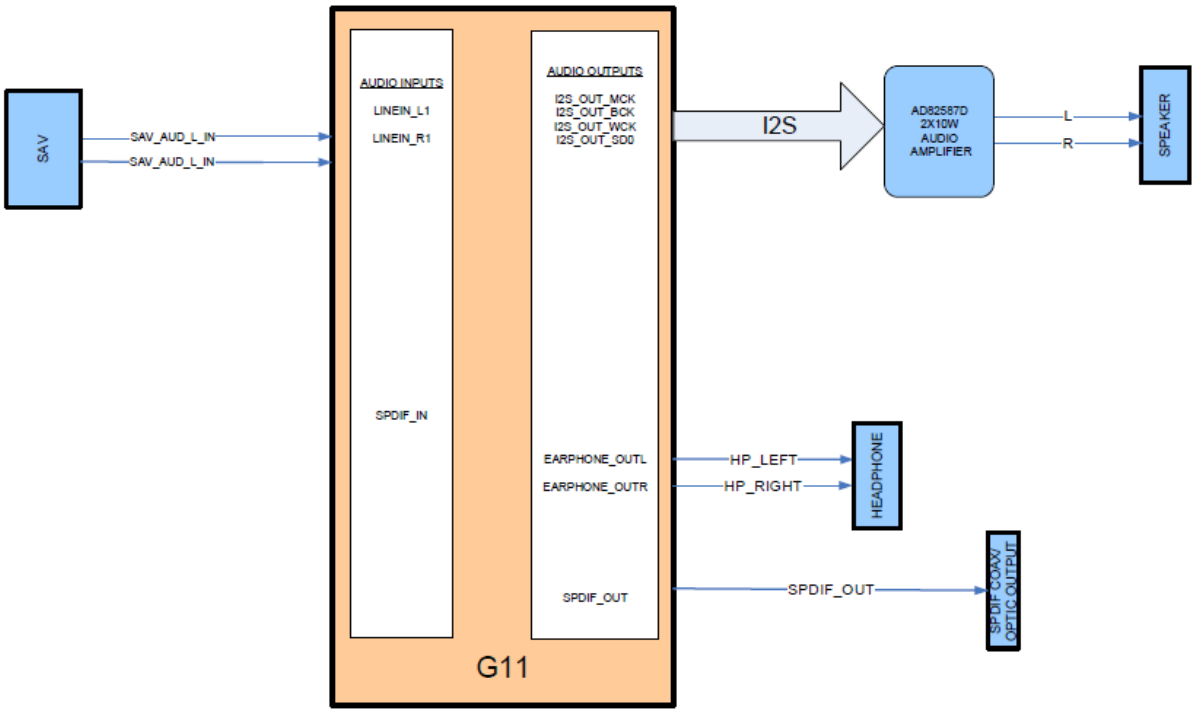


Figure 3: The block diagram of the audio part

MAIN AMPLIFIER (U123) (8W/10W/12W OPTIONS)

Description

AD82587D is a digital audio amplifier capable of driving a pair of 8 ohm, 20W or a single 4 ohm, 40W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I^2C digital control interface, the user can control AD82587D's input format selection, DRC (dynamic range control), mute and volume control functions. AD82587D has many built-in protection circuits to safeguard AD82587D from connection errors.

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting) Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  - 32kHz / 44.1kHz / 48kHz and
  - 64kHz / 88.2kHz / 96kHz and
  - 128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x,1024x Fs
  - 256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  - 128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  - 64x~256x Fs for 128kHz /176.4kHz/192kHz

- Supply voltage
  - 3.3V for digital circuit
  - 10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
  - 10W x 2ch into 8_ @ 0.16% THD+N
  - 15W x 2ch into 8_ @ 0.18% THD+N
  - 20W x 2ch into 8_ @ 0.24% THD+N
- Loudspeaker output power for Mono@ 24V
  - 20W x 1ch into 4_ @ 0.17% THD+N
  - 30W x 1ch into 4_ @ 0.2% THD+N
  - 40W x 1ch into 4_ @ 0.24% THD+N
- Sounds processing including:
  - Volume control (+24dB~-103dB, 0.125dB/step)
  - Dynamic range control
  - Power clipping
  - Channel mixing
  - User programmed noise gate with hysteresis window
  - DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage
- detection
- Power saving mode
- Dynamic temperature control

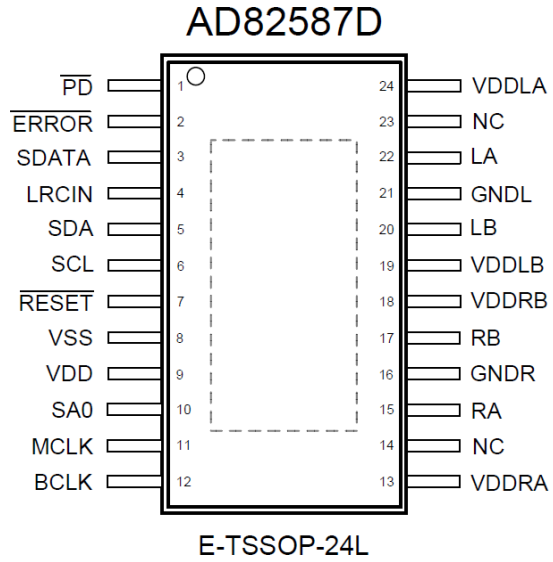


Figure 2: Pin description

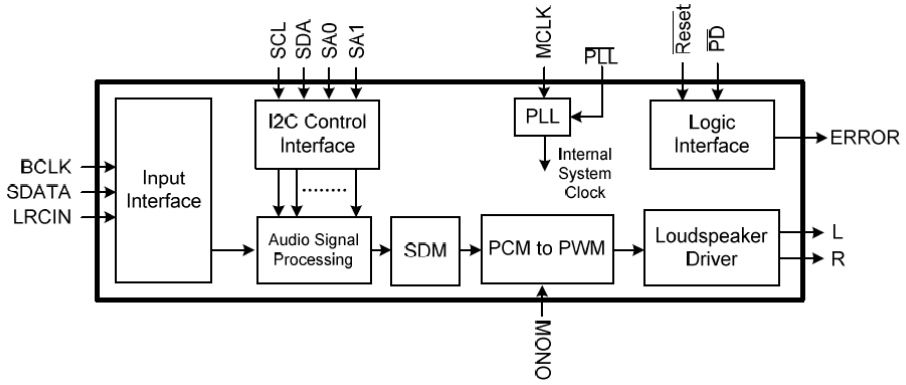


Figure 3: Functional Block Diagram

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_J	Junction Operating Temperature	0~125	°C
T_A	Ambient Operating Temperature	0~70	°C

Table 2: Recommended Operating Conditions

5. POWER STAGE

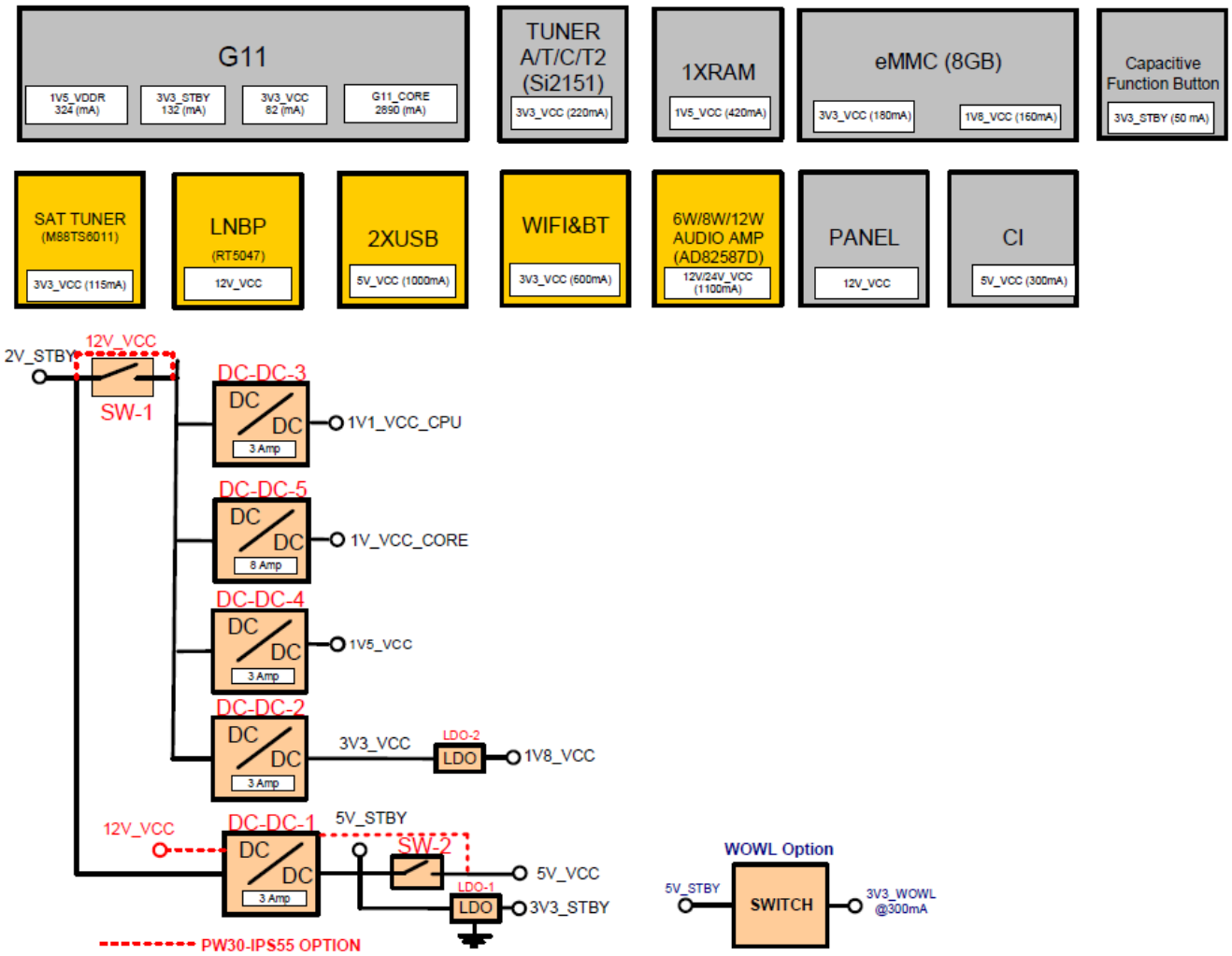


Figure 6: Power Block Diagram

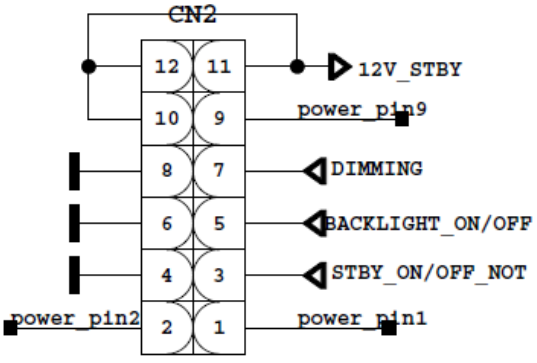


Figure 7: Power Socket and Power Options

Power socket is used for taking 12V_STBY voltage which is produced in power card. Also socket is used for giving dimming, backlight and standby signals with power card. Power socket pinning is shown in above figure.

12V_STBY is converted to several different voltages on the mainboard which are shown in below figure.

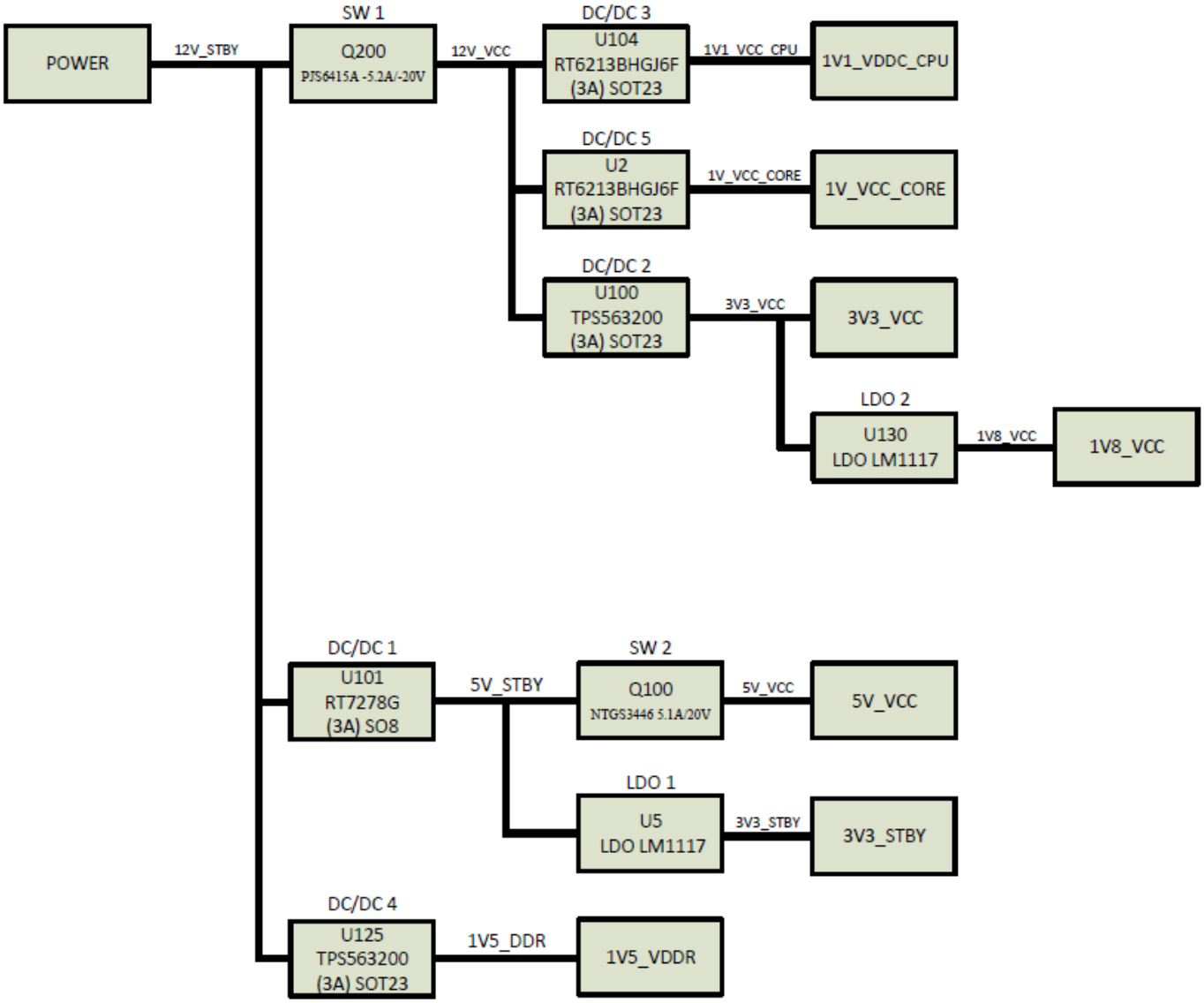


Figure 8: Power Block Diagram

List of the components:

- SW-1(Q200) → PJS6415A -5.2A/-20V
- SW-2(Q100) → NTGS3446 5.1A/20V
- DC-DC-1(U101) → RT7278G ADJ/3A
- DC-DC-2(U100) → TPS563200 ADJ/3A
- DC-DC-3(U104) → RT6213BHGJ6F ADJ/3A
- DC-DC-4(U125) → TPS563200 ADJ/3A
- DC-DC-5(U2) → RT6213BHGJ6F ADJ/3A
- LDO-1(U5) → LDO LM1117
- LDO-2(U130) → LDO LM1117

A. *PJS6415A (Q200)*

20V P-Channel Enhancement Mode MOSFET

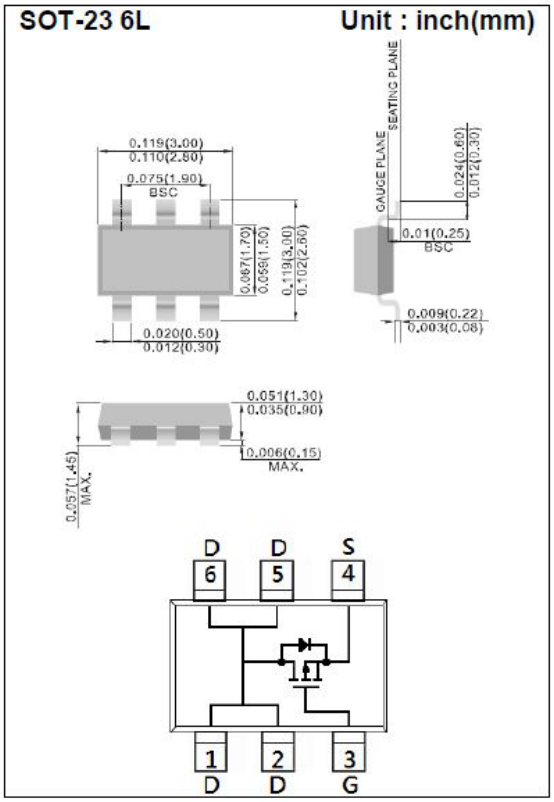
Voltage	-20 V	Current	-5.2A

Features

- $R_{DS(ON)}$, V_{GS}@-4.5V, I_D@-5.2A<46mΩ
- $R_{DS(ON)}$, V_{GS}@-2.5V, I_D@-3.0A<56mΩ
- $R_{DS(ON)}$, V_{GS}@-1.8V, I_D@-1.5A<88mΩ
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

- Case: SOT-23 6L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0005 ounces, 0.014 grams



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current		I_D	-5.2	A
Pulsed Drain Current		I_{DM}	-20.8	A
Power Dissipation	T_a=25°C	P_D	2	W
	Derate above 25°C		16	mW/°C
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C
Typical Thermal resistance - Junction to Ambient (Note 3)		$R_{\theta JA}$	62.5	°C/W

Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250uA	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250uA	-0.5	-0.74	-1.3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=-4.5V, I_D=-5.2A	-	38	46	mΩ
		V_{GS}=-2.5V, I_D=-3.0A	-	47	56	
		V_{GS}=-1.8V, I_D=-1.5A	-	68	88	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-16V, V_{GS}=0V	-	-	-1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-10V, I_D=-5.2A, V_{GS}=-4.5V (Note 1,2)	-	10	-	nC
Gate-Source Charge	Q_{gs}		-	1.7	-	
Gate-Drain Charge	Q_{gd}		-	2.4	-	
Input Capacitance	Ciss	V_{DS}=-10V, V_{GS}=0V, f=1.0MHZ	-	980	-	pF
Output Capacitance	Coss		-	100	-	
Reverse Transfer Capacitance	Crss		-	81	-	
Switching						
Turn-On Delay Time	$td_{(on)}$	V_{DD}=-10V, I_D=-5.2A, V_{GS}=-4.5V, R_G=6Ω (Note 1,2)	-	9.8	-	ns
Turn-On Rise Time	tr		-	54	-	
Turn-Off Delay Time	$td_{(off)}$		-	44	-	
Turn-Off Fall Time	tf		-	31	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	—	-	-	-2.0	A
Diode Forward Voltage	V_{SD}	I_S=-1.0A, V_{GS}=0V	-	-0.78	-1.2	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper
4. The maximum current rating is package limited

B. NTGS3446 (Q100)

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- IDSS Specified at Elevated Temperature
- Pb−Free Package is Available

Applications

- Power Management in portable and battery−powered products, i.e. computers, printers, PCMCIA cards, cellular and cordless
- Lithium Ion Battery Applications
- Notebook PC

PIN ASSIGNMENT

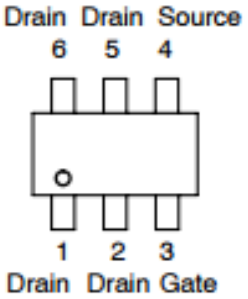


Figure 9: Pin description

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	V
Gate–to–Source Voltage	V_{GS}	±12	V
Thermal Resistance Junction–to–Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Drain Current – Continuous @ T_A = 25°C – Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 244 0.5 2.5 10	 °C/W W A A
Thermal Resistance Junction–to–Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Drain Current – Continuous @ T_A = 25°C – Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 128 1.0 3.6 14	 °C/W W A A
Thermal Resistance Junction–to–Ambient (Note 3) Total Power Dissipation @ T_A = 25°C Drain Current – Continuous @ T_A = 25°C – Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 62.5 2.0 5.1 20	 °C/W W A A
Source Current (Body Diode)	I_S	5.1	A
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	°C

Table 3: Maximum ratings

C. RT7278G (U101)

General Description

The RT7278 is a synchronous DC/DC step-down converter with Advanced Constant On-Time (ACOT™) mode control. It achieves high power density to deliver up to 3A output current from a 4.5V to 18V input supply. The proprietary ACOT™ mode offers an optimal transient response over a wide range of loads and all kinds of ceramic capacitors, which allows the device to adopt very low ESR output capacitors for ensuring performance stabilization. In addition, RT7278 keeps an excellent constant switching frequency under line and load variation and the integrated synchronous power switches with the ACOT™ mode operation provides high efficiency in whole output current load range. Cycle-by-cycle current limit provides an accurate protection by a valley detection of low side MOSFET and external soft-start setting eliminates input current surge during startup. Protection functions also include output under voltage protection, output over voltage protection, and thermal shutdown.

Features

- **ACOT™ Mode Enables Fast Transient Response**
- **4.5V to 18V Input Voltage Range**
- **3A Output Current**
- **60mΩ Internal Low Site N-MOSFET**
- **Advanced Constant On-Time Control**
- **Support All Ceramic Capacitors**
- **Up to 95% Efficiency**
- **700kHz Switching Frequency**
- **Adjustable Output Voltage from 0.765V to 8V**
- **Adjustable Soft-Start**
- **Cycle-by-Cycle Current Limit**
- **Input Under Voltage Lockout**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

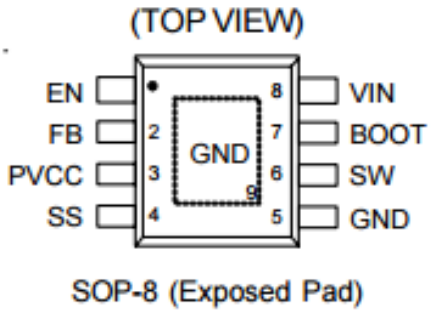


Figure 10: Pin Assignment

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable Control Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA.
2	FB	Feedback Voltage Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider. The feedback threshold voltage is 0.765V typically.
3	PVCC	Regulator Output for Internal Circuit. Connect a 1μF capacitor to GND to stabilize output voltage.
4	SS	Soft-Start Time Setting. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 3.9nF capacitor sets the soft-start period of V_{OUT} to 2.6ms.
5, 9 (Exposed Pad)	GND	Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.
6	SW	Switch Node. Connect this pin to an external L-C filter.
7	BOOT	Bootstrap Supply for High Side Gate Driver. Connect a 0.1μF or greater ceramic capacitor from BOOT to SW pins.
8	VIN	Power Input. The input voltage range is from 4.5V to 18V. Must bypass with a suitably large (≥10μF x 2) ceramic capacitor.

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	1.5	10	μA
Quiescent Current		I_Q	V_{EN} = 3V, V_{FB} = 1V	--	0.7	--	mA
Logic Threshold							
EN Input Voltage	Logic-High			2	--	18	V
	Logic-Low			--	--	0.4	
V_{FB} Voltage and Discharge Resistance							
Feedback Threshold Voltage		V_{FB}	4.5V ≤ V_{IN} ≤ 18V	0.757	0.765	0.773	V
Feedback Input Current		I_{FB}	V_{FB} = 0.8V	–0.1	0	0.1	μA
V_{PVCC} Output							
V_{PVCC} Output Voltage		V_{PVCC}	6V ≤ V_{IN} ≤ 18V, 0 < I_{PVCC} < 5mA	4.7	5.1	5.5	V
Line Regulation			6V ≤ V_{IN} ≤ 18V, I_{PVCC} = 5mA	--	--	20	mV
Load Regulation			0 < I_{PVCC} < 5mA	--	--	100	mV
Output Current		I_{PVCC}	V_{IN} = 6V, V_{PVCC} = 4V	--	110	--	mA

D. TPS563200 (U100, U125)

1 Features

- TPS562200 - 2A converter with Integrated 122 mΩ and 72 mΩ FETs
- TPS563200 - 3A converter with Integrated 68 mΩ and 39 mΩ FETs
- D-CAP2™ Mode Control for Fast Transient Response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- 650 kHz Switching Frequency
- Advanced Eco-mode™ Pulse-skip
- Low Shutdown Current Less than 10 µA
- 1% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage
- Cycle-By-Cycle Overcurrent Limit
- Hiccup-Mode Undervoltage Protection
- Non-latch OVP, UVLO and TSD Protections
- Fixed Soft Start: 1 ms

2 Applications

- Digital TV Power Supply
- High Definition Blu-ray Disc™ Players
- Networking Home Terminal
- Digital Set Top Box (STB)

3 Description

The TPS562200 and TPS563200 are simple, easy-to-use, 2 A and 3 A synchronous step-down (buck) converters in 6 pin SOT-23 package.

The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

TPS562200 and TPS563200 operate in Advanced Eco-mode, which maintains high efficiency during light load operation. The devices are available in a 6-pin 1.6mm x 2.9mm SOT (DDC) package, and specified from –40°C to 85°C of ambient temperature.

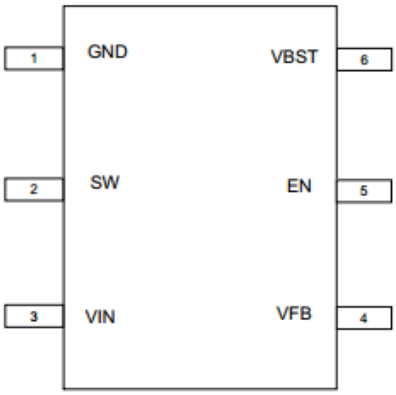


Figure 11: Pin Assignment

Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect a 0.1µF capacitor between VBST and SW pins.

Electrical Characteristics

T_J = -40°C to 150°C, VIN = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{(VIN)}$	Operating – non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5V, V_{FB} = 0.8 V	TPS562200		230	330	µA
			TPS563200		190	290	
$I_{(VINSDN)}$	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V			3	10	µA
LOGIC THRESHOLD							
$V_{EN(H)}$	EN high-level input voltage	EN		1.6			V
$V_{FN(L)}$	EN low-level input voltage	EN				0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		225	450	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE							
$V_{FB(TH)}$	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, I_O = 10mA, Eco-mode™ operation			772		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode operation		758	765	772	mV
$I_{(VFB)}$	V_{FB} input current	V_{FB} = 0.8V, T_A = 25°C			0	±0.1	µA
MOSFET							
$R_{DS(on)h}$	High side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V	TPS562200		122		mΩ
			TPS563200		68		mΩ
$R_{DS(on)l}$	Low side switch resistance	T_A = 25°C	TPS562200		72		mΩ
			TPS563200		39		mΩ
CURRENT LIMIT							
I_{ocl}	Current limit (1)	DC current, V_{OUT} = 1.05 V, L_{OUT} = 2.2 µF	TPS562200	2.5	3.2	4.3	A
		DC current, V_{OUT} = 1.05 V, L_{OUT} = 1.5 µF	TPS563200	3.5	4.2	5.3	A
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold (1)	Shutdown temperature			155		°C
		Hysteresis			35		
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
V_{OVP}	Output OVP threshold	OVP Detect			125% x Vfbth		
V_{UVP}	Output Hiccup threshold	Hiccup detect			65% x Vfbth		
$t_{HiccupOn}$	Hiccup On Time	Relative to soft-start time			1		ms
$t_{HiccupOff}$	Hiccup Off Time	Relative to soft-start time			7		ms
UVLO							
UVLO	UVLO threshold	Wake up VIN voltage		3.45	3.75	4.05	V
		Hysteresis VIN voltage		0.13	0.32	0.55	

(1) Not production tested

E. RT6213BHGJ6F (U2 – U104)

RICHTEK®

RT6213A/B

3A Peak, 18V, 500kHz, ACOT™ Step-Down Converter

General Description

The RT6213A/B is a high-efficiency, monolithic synchronous step-down DC/DC converter that can deliver up to 3A peak output current from a 4.5V to 18V input supply. The RT6213A/B adopts ACOT architecture to allow the transient response to be improved and keep in constant frequency. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. Fault conditions also include output under voltage protection, output over current protection, and thermal shutdown.

Ordering Information

RT6213A/B □□□

- Package Type
  J6F : TSOT-23-6 (FC)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- UVP Option
  H : Hiccup
- PSM/PWM
  A : PSM Mode
  B : PWM Mode

Note :

Richtek products are :

- ▸ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▸ Suitable for use in SnPb or Pb-free soldering processes.

Features

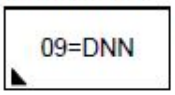
- Integrated 150mΩ/70mΩ MOSFETs
- 4.5V to 18V Supply Voltage Range
- 500kHz Switching Frequency
- ACOT Control
- 0.8V ± 1.5% Voltage Reference
- Internal Start-Up into Pre-biased Outputs
- Compact Package: TSOT-23-6 pin
- Input Under-Voltage Lockout
- Over-Current Protection and Hiccup

Applications

- Set-Top Boxes
- Portable TVs
- Access Point Routers
- DSL Modems
- LCD TVs

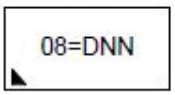
Marking Information

RT6213AHGJ6F



09= : Product Code
DNN : Date Code

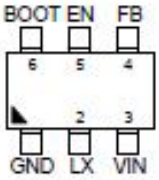
RT6213BHGJ6F



08= : Product Code
DNN : Date Code

Pin Configurations

(TOP VIEW)

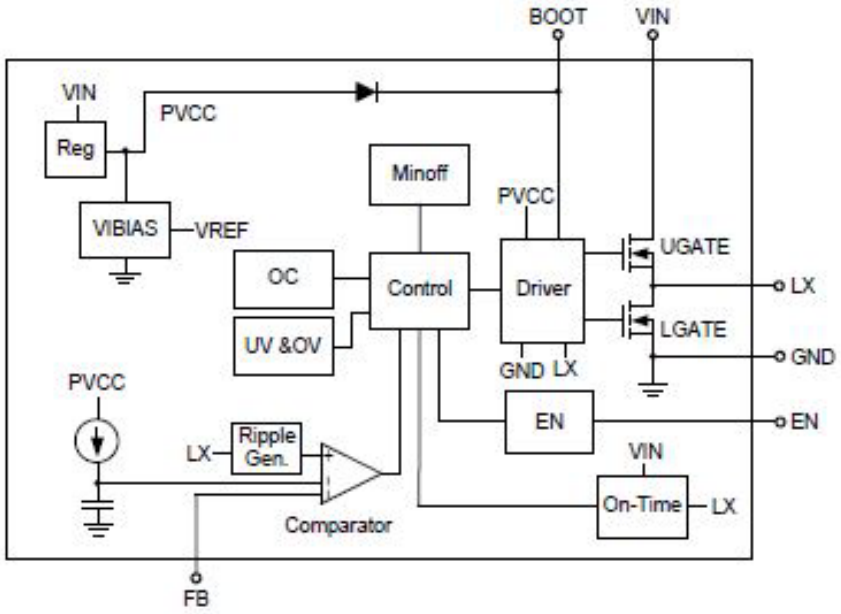


TSOT-23-6 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	System Ground. Provides the ground return path for the control circuitry and low-side power MOSFET.
2	LX	Switch Node. LX is the switching node that supplies power to the output and connect the output LC filter from LX to the output load.
3	VIN	Power Input. Supplies the power switches of the device.
4	FB	Feedback Voltage Input. This pin is used to set the desired output voltage via an external resistive divider. The feedback voltage is 0.8V typically.
5	EN	Enable Control Input. Floating this pin or connecting this pin to GND can disable the device and connecting this pin to logic high can enable the device.
6	BOOT	Bootstrap Supply for High-Side Gate Driver. Connect a 100nF or greater capacitor from LX to BOOT to power the high-side switch.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 20V
- Switch Node Voltage, LX ---------- –0.3V to (V_{IN} + 0.3V)
- BOOT Pin Voltage ---------- (V_{LX} – 0.3V) to (V_{IN} + 6.3V)
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  TSOT-23-6 (FC) ---------- 1.667W
- Package Thermal Resistance (Note 2)

  TSOT-23-6 (FC), θ_{JA} ---------- 60°C/W

  TSOT-23-6 (FC), θ_{JC} ---------- 8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 4.5V to 18V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Operating Voltage	V_{IN}		4.5	--	18	V
Under-Voltage Lockout Threshold	V_{UVLO}		3.6	3.9	4.2	
Under-Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	340	--	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.85V	--	0.5	--	mA
Soft-Start						
Soft-Start Time			--	1000	--	μS
Enable Voltage						
Enable Voltage Threshold		V_{EN} Rising	1.4	1.5	1.6	V
		V_{EN} Falling	1.18	1.28	1.38	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Voltage						
Feedback Voltage Threshold	V_{FB_TH}	$4.5V \le V_{IN} \le 18V$	0.788	0.8	0.812	V
Internal MOSFET						
High-Side On-Resistance	$R_{DS(ON)\_H}$	$V_{BOOT} - V_{LX} = 4.8V$	--	150	--	mΩ
Low-Side On-Resistance	$R_{DS(ON)\_L}$		--	70	--	
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}		--	5.8	--	A
Low-Side Switch Valley Current Limit	I_{LIM_L}		3.1	3.8	--	
Switching Frequency						
Switching Frequency	f_{OSC}		400	500	--	kHz
On-Time Timer Control						
Maximum Duty Cycle	D_{MAX}		--	86	--	%
Minimum On Time	$t_{ON(MIN)}$		--	60	--	nS
Minimum Off Time	$t_{OFF(MIN)}$		--	240	--	
Output Under Voltage and Over Voltage Protections						
OVP Trip Threshold		OVP Detect	--	125	--	%
OVP Propagation Delay			--	10	--	μS
UVP Trip Threshold		UVP Detect	45	50	55	%
		Hysteresis	--	10	--	
UVP Propagation Delay			--	5	--	μS
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. The first layer of copper area is filled θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

F. LDO LM1117 (U130, U5)

LM1117 800-mA Low-Dropout Linear Regulator

Features

- Available in 1.8 V, 2.5 V, 3.3 V, 5 V, and Adjustable Versions
- Space-Saving SOT-223 and WSON Packages
- Current Limiting and Thermal Protection
- Output Current 800 mA
- Line Regulation 0.2% (Maximum)
- Load Regulation 0.4% (Maximum)
- Temperature Range
  - LM1117: 0°C to 125°C
  - LM1117I: −40°C to 125°C

Applications

- Post Regulator for Switching DC–DC Converter
- High Efficiency Linear Regulators
- Battery Chargers
- Portable Instrumentation
- Active SCSI Termination Regulator

Description

The LM1117 is a low dropout voltage regulator with a dropout of 1.2 V at 800 mA of load current.

The LM1117 is available in an adjustable version, which can set the output voltage from 1.25 to 13.8 V with only two external resistors. In addition, it is available in five fixed voltages, 1.8 V, 2.5 V, 3.3 V, and 5 V.

The LM1117 offers current limiting and thermal shutdown. Its circuit includes a Zener trimmed bandgap reference to assure output voltage accuracy to within ±1%.

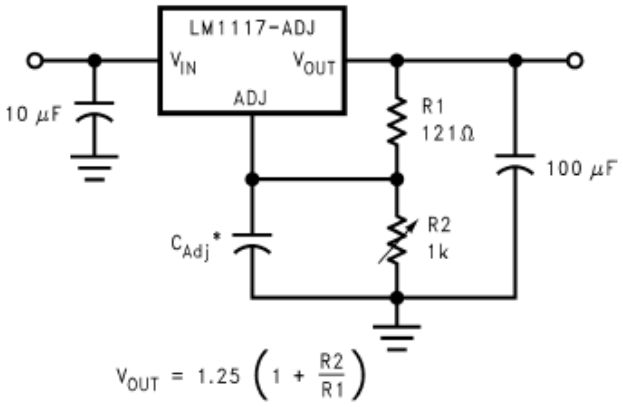
A minimum of 10-µF tantalum capacitor is required at the output to improve the transient response and stability.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM1117, LM1117I	SOT-223 (4)	6.50 mm × 3.50 mm
	TO-220 (3)	14.986 mm × 10.16 mm
	TO-252 (3)	6.58 mm × 6.10 mm
	WSON (8)	4.00 mm × 4.00 mm
	TO-263 (3)	10.18 mm × 8.41 mm

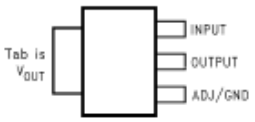
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Adjustable Output Regulator

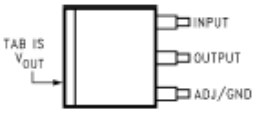


Pin Configuration and Functions

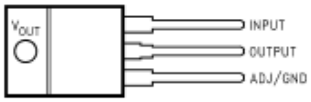
DCY Package
4-Pin SOT
Top View



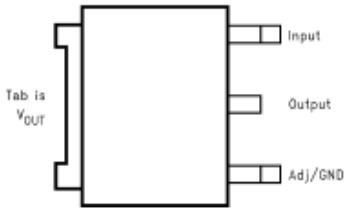
KTT Package
3-Pin TO-263
Top View



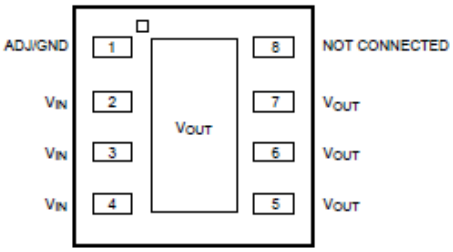
NDE Package
3-Pin TO-220
Top View



NDP Package
3-Pin TO-252
Top View



NGN Package
8-Pin WSON
Top View



When using the WSON package
Pins 2, 3 and 4 must be connected together and
Pins 5, 6 and 7 must be connected together

Pin Functions

PIN						I/O	DESCRIPTION
NAME	TO-252	WSON	SOT-223	TO-263	TO-220		
ADJ/GND	1	1	1	1	1	—	Adjust pin for adjustable output option. Ground pin for fixed output option.
V_{IN}	3	2, 3, 4	3	3	3	I	Input voltage pin for the regulator
V_{OUT}	2 , TAB	5, 6, 7, TAB	2, 4	2, TAB	2, TAB	O	Output voltage pin for the regulator

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum Input Voltage (V_{IN} to GND)			20	V
Power Dissipation(2)		Internally Limited		
Junction Temperature (T_J)(2)			150	°C
Lead Temperature	TO-220 (T) Package, 10 s		260	°C
	SOT-223 (MP) Package, 4 s		260	
Storage Temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}–T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage (V_{IN} to GND)			15	V
Junction Temperature (T_J)(1)	LM1117	0	125	°C
	LM1117I	−40	125	

(1) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}–T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

Thermal Information

THERMAL METRIC(1)		LM1117, LM1117I					UNIT
		DCY (SOT-223)	NDE (TO-220)	NDP (TO-252)	NGN (WSON)	KTT (TO-263)	
		4 PINS	3 PINS	3 PINS	8 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.6	23.8	45.1	39.3	41.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.5	16.6	52.1	31.4	44.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.4	5.3	29.8	16.5	24.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	3.1	4.5	0.3	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.3	5.3	29.4	16.7	23.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	1.5	1.3	5.6	1.3	°C/W

LM1117 Electrical Characteristics

unless otherwise specified, T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{REF}	Reference Voltage	LM1117-ADJ I_{OUT} = 10 mA, $V_{IN} – V_{OUT}$ = 2 V, T_J = 25°C		1.238	1.25	1.262	V
		LM1117-ADJ 10 mA ≤ I_{OUT} ≤ 800 mA, 1.4 V ≤ $V_{IN} – V_{OUT}$ ≤ 10 V	T_J = 25°C		1.25		
			over the junction temperature range 0°C to 125°C	1.225		1.27	
V_{OUT}	Output Voltage	LM1117-1.8 I_{OUT} = 10 mA, V_{IN} = 3.8 V, T_J = 25°C		1.782	1.8	1.818	V
		LM1117-1.8 0 ≤ I_{OUT} ≤ 800 mA, 3.2 V ≤ V_{IN} ≤ 10 V	T_J = 25°C		1.8		
			over the junction temperature range 0°C to 125°C	1.746		1.854	
		LM1117-2.5 I_{OUT} = 10 mA, V_{IN} = 4.5 V, T_J = 25°C		2.475	2.5	2.525	V
		LM1117-2.5 0 ≤ I_{OUT} ≤ 800 mA, 3.9 V ≤ V_{IN} ≤ 10 V	T_J = 25°C		2.5		
			over the junction temperature range 0°C to 125°C	2.45		2.55	
		LM1117-3.3 I_{OUT} = 10 mA, V_{IN} = 5 V T_J = 25°C		3.267	3.3	3.333	V
		LM1117-3.3 0 ≤ I_{OUT} ≤ 800 mA, 4.75 V ≤ V_{IN} ≤ 10 V	T_J = 25°C		3.3		
			over the junction temperature range 0°C to 125°C	3.235		3.365	
		LM1117-5.0 I_{OUT} = 10 mA, V_{IN} = 7 V, T_J = 25°C		4.95	5	5.05	V
		LM1117-5.0 0 ≤ I_{OUT} ≤ 800 mA, 6.5 V ≤ V_{IN} ≤ 12 V	T_J = 25°C		5		
			over the junction temperature range 0°C to 125°C	4.9		5.1	

ΔV_{OUT}	Line Regulation(3)	LM1117-ADJ I_{OUT} = 10mA, 1.5V ≤ V_{IN}-V_{OUT} ≤ 13.75V	T_J = 25°C	0.035%	
			over the junction temperature range 0°C to 125°C	0.2%	
		LM1117-1.8 I_{OUT} = 0 mA, 3.2 V ≤ V_{IN} ≤ 10 V	T_J = 25°C	1	mV
			over the junction temperature range 0°C to 125°C	6	
		LM1117-2.5 I_{OUT} = 0 mA, 3.9 V ≤ V_{IN} ≤ 10 V	T_J = 25°C	1	mV
			over the junction temperature range 0°C to 125°C	6	
		LM1117-3.3 I_{OUT} = 0 mA, 4.75 V ≤ V_{IN} ≤ 15 V	T_J = 25°C	1	mV
			over the junction temperature range 0°C to 125°C	6	
		LM1117-5.0 I_{OUT} = 0 mA, 6.5 V ≤ V_{IN} ≤ 15 V	T_J = 25°C	1	mV
			over the junction temperature range 0°C to 125°C	10	
ΔV_{OUT}	Load Regulation(3)	LM1117-ADJ V_{IN} – V_{OUT} = 3 V, 10 ≤ I_{OUT} ≤ 800 mA	T_J = 25°C	0.2%	
			over the junction temperature range 0°C to 125°C	0.4%	
		LM1117-1.8 V_{IN} = 3.2 V, 0 ≤ I_{OUT} ≤ 800 mA	T_J = 25°C	1	mV
			over the junction temperature range 0°C to 125°C	10	
		LM1117-2.5 V_{IN} = 3.9 V, 0 ≤ I_{OUT} ≤ 800 mA	T_J = 25°C	1	mV
			over the junction temperature range 0°C to 125°C	10	
		LM1117-3.3 V_{IN} = 4.75 V, 0 ≤ I_{OUT} ≤ 800 mA	T_J = 25°C	1	mV
			over the junction temperature range 0°C to 125°C	10	
		LM1117-5.0 V_{IN} = 6.5 V, 0 ≤ I_{OUT} ≤ 800 mA	T_J = 25°C	1	mV
			over the junction temperature range 0°C to 125°C	15	

(1) All limits are ensured by testing or statistical analysis.
(2) Typical Values represent the most likely parametric normal.
(3) Load and line regulation are measured at constant junction room temperature.

unless otherwise specified, T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
$V_{IN} - V_{OUT}$	Dropout Voltage(4)	I_{OUT} = 100 mA	T_J = 25°C		1.1		V
			over the junction temperature range 0°C to 125°C			1.2	
		I_{OUT} = 500 mA	T_J = 25°C		1.15		V
			over the junction temperature range 0°C to 125°C			1.25	
		I_{OUT} = 800 mA	T_J = 25°C		1.2		V
			over the junction temperature range 0°C to 125°C			1.3	
I_{LIMIT}	Current Limit	$V_{IN} - V_{OUT}$ = 5 V, T_J = 25°C		800	1200	1500	mA
	Minimum Load Current(5)	LM1117-ADJ V_{IN} = 15 V	T_J = 25°C		1.7		mA
			over the junction temperature range 0°C to 125°C			5	
	Quiescent Current	LM1117-1.8 $V_{IN} \le$ 15 V	T_J = 25°C		5		mA
			over the junction temperature range 0°C to 125°C			10	
		LM1117-2.5 $V_{IN} \le$ 15 V	T_J = 25°C		5		mA
			over the junction temperature range 0°C to 125°C			10	
		LM1117-3.3 $V_{IN} \le$ 15 V	T_J = 25°C		5		mA
			over the junction temperature range 0°C to 125°C			10	
		LM1117-5.0 $V_{IN} \le$ 15 V	T_J = 25°C		5		mA
			over the junction temperature range 0°C to 125°C			10	
	Thermal Regulation	T_A = 25°C, 30-ms pulse			0.01	0.1	%/W
	Ripple Regulation	f_{RIPPLE} = 1 20 Hz, $V_{IN} - V_{OUT}$ = 3 V V_{RIPPLE} = 1 V_{PP}	T_J = 25°C		75		dB
			over the junction temperature range 0°C to 125°C	60			
	Adjust Pin Current	T_J = 25°C			60		µA
		over the junction temperature range 0°C to 125°C				120	
	Adjust Pin Current Change	10 ≤ I_{OUT} ≤ 80 0mA, 1.4 V ≤ $V_{IN} - V_{OUT} \le$ 10 V	T_J = 25°C		0.2		µA
			over the junction temperature range 0°C to 125°C			5	
	Temperature Stability				0.5%		
	Long Term Stability	T_A = 125°C, 1000 Hrs			0.3%		
	RMS Output Noise	(% of V_{OUT}), 10 Hz ≤ f ≤ 10 kHz			0.003%		

(4) The dropout voltage is the input/output differential at which the circuit ceases to regulate against further reduction in input voltage. It is measured when the output voltage has dropped 100 mV from the nominal value obtained at $V_{IN} = V_{OUT}$ + 1.5 V.
(5) The minimum output current required to maintain regulation.

6. MICROCONTROLLER

MTK G11 (U1)

Description

The MSD94BDX4 is MediaTek's most state-of-the-art solution for flat panel integrated digital television products. Building on the success of MediaTek's current solutions, the MSD94BDX4 hosts the most advanced picture processing engine, ACE^{PRO}, for all the Experts in various fields of TV video quality tuning to develop the state-of-the-art TV and DTV system.

ACE^{PRO}, the Professional Edition of MediaTek color processor, includes all MediaTek's successful color-tuning tools and a newly added multi-dimensional color/sharpening/NR formula that can quickly reflect subtle or sudden changes in even darker, brighter or mixture scenes. With this ultimate color processor, a specially designed color remapping system for modern wider gamut displays and an easy-to-use color-tool UI, developers can quickly and easily identify PQ characteristic from the most high-end panel models to the most conventional panel models.

The MSD94BDX4 integrates DTV/multi-media all-purpose AV decoder ATSC/QAM, ISDB-T, DVB-T, DVB-T2, DVB-S, DVB-S2, DVB-C demodulator, VIF demodulator and Sound/Video processor into a single device. This allows the overall BOM to be reduced significantly making the MSD94BDX4 a very cost effective multi-media DTV solution.

The MSD94BDX4 enables feature-rich products that bring differentiation to the iDTV market. By the use of AV decoder capable of decoding a plethora of high definition content with USB 2.0 connectivity and a powerful CPU and advanced graphic engine, an MSD94BDX4 based system can provide a high quality networking application and media-center experience.

For standard users, the MSD94BDX4 provides multi-standard analog TV supported with adaptive 3D video decoding and VBI data extraction. The build-in audio decoder is capable of decoding FM, AM, NICAM, A2, BTSC and sound standards. The MSD94BDX4 supplies all the necessary A/V inputs and outputs to complete a receiver design including a multi-port HDMI receiver and component video ADC. All input selection multiplexed for video and audio are integrated, including full SCART support with CVBS output.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MSD94BDX4 has an ultra low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

Features

Attention Please: Under the technology license agreement between MediaTek and Dolby/DTS/Microsoft/THAT, MediaTek is obliged not to provide samples that incorporate Dolby/DTS/Microsoft/THAT technology to any third party who is not a qualified licensee of Dolby/DTS/Microsoft/THAT respectively.

MSD94BDX4 a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU.

Key features includes,

1. *Combo Front-End Demodulators*
2. *A Multi-Standard A/V Format Decoder*
3. *The ACE^{PRO} Video Processor*
4. *Home Theater Sound Processor*
5. *Rich internet connectivity and completed digital home network solution*
6. *Dual-stream decoder for 3D contents*
7. *Multi-Purpose CPU for OS and Multimedia*
8. *Security Engine and TEE*
9. *Peripheral and Power Management*
10. *Embedded DRAM*

- High Performance Micro-processor
  - ARM Coretex Advanced quad-core CPU
  - 32KB/32KB I/D cache
  - 512KB L2 cache
- Transport Stream De-multiplexer
  - Supports two parallel TS interfaces, with or without sync signal
  - Maximum TS data rate is 140Mbit/s for serial and 24MByte/s for parallel
  - 72 general purpose PID filters and 64 section filters for transport stream de-multiplexer
  - Supports time-shifting function
  - Supports 3DES/DES and AES decrypted cipher engine
- MPEG-2 Video Decoder
  - ISO/IEC 11172-2 MPEG-1 video format decoding
  - ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
  - Supports resolution up to HDTV (1080p60, 1080i, 720p) and SDTV
  - Supports dual stream decoding for 3D content
- MPEG-4 Video Decoder
  - ISO/IEC 14496-2 MPEG-4 ASP video decoding up to HD level
  - Supports resolutions up to HDTV (1080p@60fps)
  - Supports FLV version1 video format decoding
  - Supports dual stream decoding for 3D content
- AVC/H.264 Video Decoder
  - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 4.2) video decoding
  - Supports resolution up to 1920x1080@60fps
  - Supports bitrate up to 62.5Mbps, the upper limit of level 4.2
  - Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
  - Supports SVAF 2ES (for Dual Decode)
  - Supports MVC 3D decoding upto 1080p@30fps
- AVS/AVS+ Video Decoder[Optional]
  - Supports Broadcasting profile, level 6.0.1.08.60 (AVS+)
  - Supports Jizhun profile, level 6.0

- Supports bitrate up to 50Mbps
- Supports resolution up to 1920x1080@60fps
- Supports dual stream decoding

■ RealMedia Video Decoder Optional
- Supports RV8, RV9, RV10 decoders
- Supports file formats with RM and RMVB
- Supports maximum resolution up to 1080p@30fps
- Supports Picture Re-sampling
- Supports in-loop de-block for B-frame

■ AVC/H.264 Video Encoder
- Supports H.264 encoding, Main Profile, level 4.1
- Maximum output frame-rate/resolution: 1920x1080@30fps, 1280x720@60fps
- Supports MVs: 16x16, 16x8, 8x16, 8x4, 4x8, 4x4
- Supports up to quarter-pel
- Supports up to two reference frames

■ HEVC/H.265 Video Decoder
- Supports HEVC/H.265 video decoding
- Supports Main/Main-10 profile & Scalable Main/Scalable Main-10 profile, level 4.1, high tier
- Supports 8-bit/10-bit color depth
- Supports resolution up to 1920x1080@60fps
- Supports max bitrate upto 50 Mbps

■ Hardware PNG / GIF Decoder
- Supports up to 8192 x 8192 (per channel 8 bits), or 4096 x 8192(per channel 16 bits) pixel image
- PNG format 1bpp/2bpp/4bpp/8bpp index(palette) mode support
- PNG transparency mode support interlaced / non-interlaced GIF support
- ARGB8888, RGB565, YUV422(YUYV),YUV422(YVYU),gray, gray with alpha output format support

■ Hardware JPEG Decoder
- Supports upto 640x480@30fps
- Supports formats: 422/411/420/444/422T
- Supports scaling down ratios: 1/2x1/2, 1/4x1/4, 1/8x1/8
- Supports both color and grayscale pictures
- Supports sequential mode, single scan
- Supports programmable Region of Interest (ROI)
- Following the file header scan the hardware decoder fully handles the decode process

■ VC-1 Video Decoder Optional
- Supports SMPTE-421M (VC1 video) decoding up to AP@L3 (2048x1024p60)
- Supports dual stream decoding for 3D content
- Supports upto 1920x1080p60*2 or 1920x1080p30*4

■ NTSC/PAL/SECAM Video Decoder
- Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
- Automatic standard detection
- Motion adaptive 3D comb filter
- Two configurable CVBS & Y/C S-video inputs
- Supports Teletext, Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), V-chip and SCTE

■ Multi-Standard TV Sound Processor
- Supports BTSC/A2 demodulation
- Supports NICAM/FM/AM demodulation
- Supports MTS Mode Mono/Stereo/SAP in BTSC mode
- Supports Mono/Stereo/Dual in A2/NICAM mode
- Built-in audio sampling rate conversion (SRC)
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls

- Advanced sound processing options available, for example: Dolby[1], DTS[2], DBX-TV[3]
- Supports digital audio format decoding: MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3/AC-4) Optional ,AAC-LC, HE-AAC, WMA, WMA9 Pro, and Supports Optional Dolby Digital Plus, Dolby Pulse, and MS11/MS12 multistream decoder, including Dolby Digital Encoder for trans-coding streams to Dolby Digital 5.1 (DDCO), DTS M6 multistream decoder/encoder
- Supports Audio Description
- Supports MPEG audio encoding
- Supports time-shifting PVR
- Supports programmable delay for audio/video synchronization

■ Audio Interface
- Two L/R audio line-inputs
- Two L/R outputs for main speakers and additional line-outputs
- Supports stereo headphone driver
- I2S digital audio output
- S/PDIF digital audio output and input
- Support HDMI receiver ARC function

■ VP8 Video Decoder
- Supports Google VP8 decoder
- Supports resolution up to 1920x1080@60fps
- Supports maximum bitrate upto 50Mbps

■ VP9 Video Decoder
- Supports Google VP9 decoder
- Supports 4:2:0 subsampling and 8bit/10bit color depth
- Supports max resolution and frame rate 1920x1080@60fps
- Supports max bitrate upto 40Mbps

■ Analog RGB Compliant Input Ports
- Two analog ports support up to 1080P
- Support PC RGB input up to SXGA@75Hz
- Support HDTV RGB/YPbPr/YCbCr
- Support Composite Sync and SOG (Sync-on-Green)
- Automatic color calibration

■ Analog RGB Auto-Configuration & Detection
- Auto input signal format and mode detection
- Auto-tuning function including phasing, positioning, offset, gain
- Sync Detection for H/V Sync

■ DVI/HDCP/HDMI Compliant Input Ports
- Three HDMI/DVI Input ports
- HDMI 1.4a Compliant
- iSwitch for fast HDMI switching
- HDCP 1.4/2.2 Compliant
- 225MHz @ 1080P 60Hz input with 12-bit Deep-color support
- Support HDMI CEC
- Support HDMI 1.4a 3D format input
- Support HDMI UHD input down-scaling to FHD
- Support HDMI ARC
- Single link DVI 1.0 compliant
- Robust receiver with excellent long-cable support
- Support embedded HDCP 1.4 Key
- Support external HDCP 2.2 key

■ High Performance Video Processor
- Video Processing Engine
  - Supports up to FHD@60p
  - 10-/12-bit Internal Data Processing
  - Dual-Engine Architecture supporting PIP/PBP
  - Arbitrary Frame Rate Conversion
- Video Care Technology
  - Video Line Broken Artifact Detection and Removal
- Fully Programmable Multi-Function Scaling Engine

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[1] Trademark of Dolby Laboratories

[2] Trademark of DTS, Inc.

Optional Please see Ordering Guide for details.

- High-Tap Filters with Programmable Parameter
- An advanced Zoom Algorithm providing Aliasing/Ringing Suppression
- Nonlinear Video Scaling supports various modes including Panorama
- Supports Dynamic Scaling for RM, VC-1[Optional]
- Fully Programmable Zoom Ratios for Up/Down Scaling
- Independent Horizontal and Vertical Zoom

- Deinterlacer
  - Motion Compensated Video Deinterlacing with Motion Object Stabilizer
  - Motion Adaptive Deinterlacer
  - Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal
  - Automatic 3:2/2:2/M:N Pull-Down Detection and Recovery
- Genuine 3D
  - Supports Mandatory 3D Format
- Motion Frame Rate Conversion
  - Supports Frame Repeat Frame Rate Conversion
- Backlight Technology
  - Programmable Light Spread Profile
  - Content Adaptive LCD Backlight Control
- High-Dynamic-Range
  - Supports SMPTE ST-2084 / ST-2086
  - Supports ARIB STD-B67 (Hybrid Log Gamma)
  - Support ITU-R BT.2100
  - HDR plus Technology with Standard HDR Ready
- Response Time Compensation
  - Supports Overdrive Technology

■ Professional PQ Engine

- UltraClear
  - MPEG Artifact Removal
    - ✧ Adaptive Block Noise Reduction
    - ✧ Advanced Mosquito Noise Cancellation
  - UltraClear Noise Reduction
    - ✧ 3D Motion-Estimation Temporal Filtering
  - 3D Noise Reduction
    - ✧ 3D Temporal Noise Reduction for Lousy Air/Cable Input
    - ✧ Cross-Color Suppression Technology
- S-Powers
  - Video Enhancement Processor
    - ✧ Advanced 3D Independent Multi-Band Control Sharpness Technology
    - ✧ Advanced Video Enhancement Algorithm provides Aliasing/Ringing Suppression
    - ✧ Supports Chroma Transient Improvement
    - ✧ Content Adaptive Contrast Enhancement with Chroma Compensated
  - Super Resolution
    - ✧ Local Detail Enhancement
    - ✧ Multi-Directional Jagged Compensation Technology
- MACE
  - Advanced Color Engine
    - ✧ 3D Independent and Accurate Multi-Adaptive Color Manager
    - ✧ Color Stain Removal Technology
  - Standard Color Format and Processing
    - ✧ Fully Programmable Input/Output CSC
    - ✧ BT601, BT709, BT2020 (CL/NCL)
    - ✧ xvYCC601, xvYCC709
    - ✧ AdobeRGB, AdobeYCC601
    - ✧ sRGB, sYCC601
    - ✧ Fully Programmable 12-bit RGB Gamma
  - Gamut Mapping
    - ✧ Nonlinear/Linear RGB Domain Gamut Mapping
    - ✧ Supports 2D Gamut Mapping
    - ✧ The 3rd Generation 3D Gamut Mapping Engine

- Output Interface
  - Single/Dual link 10 bit LVDS output
  - Supports panel resolution up to Full HD 1920x1080@ 60Hz (LVDS 2ch)
  - Supports TCON: mini-LVDS 2-ch interface, panel resolution up to Full HD @ 60Hz
  - Supports TCON:EPI interface, panel resolution up to Full HD @ 60Hz
  - Support TTL output, update to 1920x1080@ 60Hz
  - Supports programmable timing controller
  - Supports dithering options
  - Spread spectrum output frequency for EMI suppression
  - Supports 60Hz 3D polarizd panel (line interleave)
  - Supports Cinema output mode
- CVBS Video Encoder
  - Supports all NTSC/PAL TV Standard
  - Stand-alone scaling engine
  - Programmable Hue, Contract, Brightness
  - Supports TTX/CC/WSS output
- CVBS Video Outputs
  - Allows CVBS output from CVBS video encoder
  - Supports CVBS bypass output
- 2D Graphics Engine
  - Hardware Graphics Engine for responsive interactive applications
  - Supports point draw, line draw, rectangle draw/fill and text draw
  - Supports BitBlt, stretch BitBlt, italic Bitblt, Mirror BitBlt and rotate BitBlt
  - Supports alpha-blending operation
  - Supports source/destination color key and alpha key
  - Supports dither
  - Supports color space conversion and format transformation
  - Raster Operation (ROP)
  - Supports DFB and Porter-Duff operation
- 3D Graphics Engine
  - Powerful Multi-core Mali GPU
  - Supports OpenGL ES 1.1/2.0
  - Supports OpenGL VG 1.1
- VIF Demodulator
  - Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards.
  - Support low IF architecture
  - Audio/Video internal dual-path processor
  - Locking range improvement
- ATSC/QAM Demodulator
  - ATSC A/53 compliant 8VSB
  - ITU-T J.83 Annex B, SCTE DVS-031 compliant 64/256QAM receiver
  - 2010 - A74 compliant
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - Integrated deinterleaver RAM for Level 1 J =1 and Level 2 J= 1,2,3.4
  - Supports LIF interfaces
  - I2C repeater for tuner control from backend host controller
- ISDB-T Demodulator
  - Compliant with ISDB-T ARIB STD-B31
  - Compliant with ISDB-Tsb ARIB STD-B29
  - Supports all modes defined in ISDB-T spec
  - Supports all guard ratios: 1/4, 1/8, 1/16, 1/32
  - 42ms/channel, excluding AGC time and PLL sync
  - Support LIF interfaces
  - I2C repeater for tuner control from backend host controller
  - Impulse-noise suppression
  - Phase noise compensation
  - Outside-GI performance improvement
  - CNR performance improvement

- DVB-C Demodulator
  - Compliant with ITU J.83 Annex A/C DVB-C (EN 300 429)
  - Supports 1-7.2 M Baud symbol rate
  - Automatic blind channel scan (constellation and symbol rate)
  - Supports LIF interfaces
  - IIS performance improvement
- DVB-T Demodulator
  - Compliant with DVB-T (ETSI EN 300 744)
  - Nordig 2.2.2, D-book 7.0 compliant
  - Accept low IF inputs in 6, 7, 8MHz channel bandwidths
  - Supports all guard intervals (1/32 to 1/4)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM)
  - Ultra fast automatic blind UHF/VHF channel scan
  - Optimized for SFN channels with pre/post-cursive echoes inside/outside the guard
  - Phase-Noise suppression
  - Impulse-Noise suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - CNR performance improvement
  - Outside-GI performance improvement
- DVB-T2 Demodulator
  - Compliant with DVB-T2 (ETSI EN 302 755) v1.3.1, T2-base & T2-Lite profile
  - Compliant with DVB-T2 (ETSI EN 302 755) v1.3.1, T2-base & T2-Lite profile
  - Nordig Unified 2.2.2, D-Book 7.0 compliant
  - Supports all guard intervals (1/128 to 1/4)
  - Supports all FFT modes from 1K to 32K
  - Supports all long and short block code rates (1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 2/5, 1/3)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM, 256-QAM)
  - Transmit diversity (MISO) support
  - Supports all scattered pilot patterns (PP1 to PP8)
  - Supports rotated and non-rotated constellations
  - Supports single and multiple PLPs
  - Accept low IF inputs in 1.7, 5, 6, 7, 8MHz channel bandwidths
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - Outside GI improvement
  - Locking time improvement
- DVB-S Demodulator
  - Compliant with DVB-S (ETSI EN 300 421)
  - Data Rate: 1-70 Msps
  - Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
  - Carrier frequency acquisition range: 5MHz
  - Fast automatic blind scan of symbol rates and carrier frequencies
  - Equalizer compensates for channel impairment
  - DiSEqC™ 2.0 compatible with LNB controller
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Novel carrier recovery algorithms for tracking and compensating large phase noises
  - Integrated FEC decoders for near Shannon limit performances
  - Integrated signal quality and BER monitors
  - Improved CNR performance
- DVB-S2 Demodulator
  - Compliant with DVB-S2 (ETSI EN 302 307)
  - Data Rate: 1-70 Msps
  - Constellations: QPSK , 8PSK
  - QPSK Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10

- 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10
- Roll-off factors for pulse shaping: 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqC™ 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

■ Connectivity

- Two USB 2.0 host ports & one USB 2.0 OTG port
- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
- Built-in 10/100Mbps Ethernet PHY Interface

■ Miscellaneous

- DRAM interface supporting 32-bit DDR3 and 32-bit DDR4(optional)
- Supports RTC
- Supports Common Interface for conditional access support
- Bootable SPI interface with serial flash support
- Parallel interface for external parallel eMMC flash (optional) and NAND flash support
- Power control module with ultra low power MCU available in standby mode
- 577-ball BGA package
- Operating Voltages: 1.5V (DDR3), 1.2V/2.5V(DDR4), 3.3V (I/O and analog)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}	3.14	3.3	3.46	V
1.5V Supply Voltages (DDR3)	V_{VDD_15}	1.43	1.5	1.57	V
1.22V Supply Voltages (DDR4)	V_{VDD_122}	1.19	1.22	1.25	V
2.5V Supply Voltages (DDR4)	V_{VDD_25}	2.38	2.5	2.62	V
Core Supply Voltages	V_{VDD_core}	0.921	0.95 (VID case0)	0.978	V
		0.97	1.00 (VID case1)	1.03	V
CPU Supply Voltages	V_{VDD_cpu}	0.921	0.95 (VID case0)	0.978	V
		0.97	1.00 (VID case1)	1.03	V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Table 4: Recommended operating condition

7. 1.5GB DDR3 SDRAM

NANYA 256MX16 NT5CB256M16ER-FL 2133 (U113)

Description

Basic Functionality

The DDR3(L) SDRAM is a high-speed dynamic random access memory internally configured as an eight-bank DRAM. The DDR3(L) SDRAM uses an 8n prefetch architecture to achieve high speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3(L) SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3(L) SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A15 select the row). The address bit registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3(L) SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

Features

- **Basis DDR3 Compliant**
  - 8n Prefetch Architecture
  - Differential Clock(CK/$\overline{CK}$) and Data Strobe(DQS/$\overline{DQS}$)
  - Double-data rate on DQs, DQS and DM
- **Data Integrity**
  - Auto Self Refresh (ASR) by DRAM built-in TS
  - Auto Refresh and Self Refresh Modes
- **Power Saving Mode**
  - Power Down Mode
- **Signal Integrity**
  - Configurable DS for system compatibility
  - Configurable On-Die Termination
  - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240 ohm ± 1%)
- **Signal Synchronization**
  - Write Leveling via MR settings [5]
  - Read Leveling via MPR
- **Interface and Power Supply**
  - SSTL_15 for DDR3:VDD/VDDQ=1.5V(±0.075V)
  - SSTL_135[2] for DDR3L:VDD/VDDQ=1.35V(-0.067/+0.1V)

AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter		Rating			Unit	Note
			Min.	Typ.	Max.		
VDD	Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6,7
VDDQ	Supply Voltage for Output	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6,7

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.

2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

3. Maximun DC value may not be great than 1.425V.The DC value is the linear average of VDD/ VDDQ(t) over a very long period of time (e.g., 1 sec).

4. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.

5. Under these supply voltages, the device operates to this DDR3L specification.

6. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation.

7. VDD= VDDQ= 1.35V (1.283 – 1.45V)

Backward compatible to VDD= VDDQ= 1.5V ±0.075V

Supports DDR3L devices to be backward com-patible in 1.5V applications

Programmable Functions

- **CAS Latency (6/7/8/9/10/11/13/14)**
- **CAS Write Latency (5/6/7/8/9/10)**
- **Additive Latency (0/CL-1/CL-2)**
- **Write Recovery Time (5/6/7/8/10/12/14/16)**
- **Burst Type (Sequential/Interleaved)**
- **Burst Length (BL8/BC4/BC4 or 8 on the fly)**
- **Self RefreshTemperature Range(Normal/Extended)**
- **Output Driver Impedance (34/40)**
- **On-Die Termination of Rtt_Nom(20/30/40/60/120)**
- **On-Die Termination of Rtt_WR(60/120)**
- **Precharge Power Down (slow/fast)**

Options

- **Speed Grade (CL-TRCD-TRP) [1]**
  - 2133 Mbps / 14-14-14
  - 1866 Mbps / 13-13-13
  - 1600 Mbps / 11-11-11
- **Temperature Range (T_c) [3]**
  - Commercial Grade = 0℃~95℃
  - Quasi Industrial Grade (-T) = -40℃~95℃
  - Industrial Grade (-I) = -40℃~95℃

- **Speed Grade (CL-TRCD-TRP) [1]**
  Lead-free RoHS compliance and Halogen-free

TFBGA Package	Length x Width (mm)	Ball pitch (mm)
78-Ball	8.00 x 10.50	0.80
96-Ball	8.00 x 13.00	0.80

- **Density and Addressing**

Organization	512Mb x 8	256Mb x 16
Bank Address	BA0 – BA2	BA0 – BA2
Auto precharge	A10 / AP	A10 / AP
BL switch on the fly	A12 / $\overline{BC}$	A12 / $\overline{BC}$
Row Address	A0 – A15	A0 – A14
Column Address	A0 – A9	A0 – A9
Page Size	1KB	2KB
tREFI(us) [3]	*Tc*<=85℃:7.8, *Tc*>85℃:3.9	
tRFC(ns) [4]	260ns	

NOTE 1 Please refer to ordering information for the detail.
NOTE 2 1.35V DDR3L are backward compatible to 1.5V DDR3 parts. Please refer to operating frequency table
NOTE 3 If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9us interval refresh rate. Extended SRT or ASR must be enabled.
NOTE 4 Violating tRFC specification will induce malfunction.
NOTE 5 Only Support prime DQ's feedback for each byte lane.
NOTE 6 When operate above 95℃ ,AC/DC will be derated.

8. 8GB EMMC

SAMSUNG EMMC 8GB KLM8G1GETF-B041 BGA153 (U128)

Description

SAMSUNG eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a sim-ple read and write to memory using MMC protocol v5.1 which is a industry standard. eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply voltage (VDD or VCCQ) is supported for the MMC controller. SAMSUNG eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance. There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market. The embedded flash management software or FTL(Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

Key Features

- Embedded MultiMediaCard Ver. 5.1 compatible.
- SAMSUNG eMMC supports features of eMMC5.1 which are defined in JEDEC Standard

- Major Supported Features : HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types

- Non-supported Features : Large Sector Size (4KB)

- Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems)
- Data bus width : 1bit (Default), 4bit and 8bit
- MMC I/F Clock Frequency : 0 ~ 200MHz
  MMC I/F Boot Frequency : 0 ~ 52MHz
- Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)
- Power : Interface power →VCCQ(1.70V ~ 1.95V), Memory power → VCC(2.7V ~ 3.6V)

Item	Min	Max	Unit
V_{CCQ}	1.70	1.95	V
V_{CC}	2.7	3.6	V
V_{SS}	-0.5	0.5	V

Table 5: Supply Voltage

9. USB INTERFACE

USB POWER SWITCH ADJ SAFE TPS25221 SOT23-6 (U117-U109)

1 Features

- 2.5-V to 5.5-V $V_{OPERATING}$
- Pin-to-Pin with TI Switch Portfolio
- 2-A I_{CONT_MAX}
- 0.277-A to 2.7-A Adjustable I_{LIMIT} (±10% at 2.7 A)
- 70-mΩ (typical) R_{ON}
- 2-µs Short Circuit Response
- 8-ms Fault Reporting Deglitch
- Reverse Current Blocking (when disabled)
- Built-In Soft Start
- UL 60950 and UL 62368 Recognition Pending
- 15-kV ESD Protection per IEC 61000-4-2 (with external capacitance)

2 Applications

- USB Ports/Hubs, Laptops, Desktops
- High-Definition Digital TVs
- Set Top Boxes
- Optical Socket Protection

3 Description

The TPS25221 is intended for applications such as USB where heavy capacitive loads and short circuits may be encountered. The programmable current-limit threshold maybe set between 277 mA and 2.7 A (typical) using an external resistor. Current-limit accuracy as tight as ±10% can be achieved at the higher current-limit settings. The power-switch rise and fall times are controlled to minimize current surges during turn on and turn off.

The TPS25221 limits output current to the programmed level when the output load attempts to exceeds the current-limit threshold. The $\overline{FAULT}$ output asserts low during overcurrent conditions.

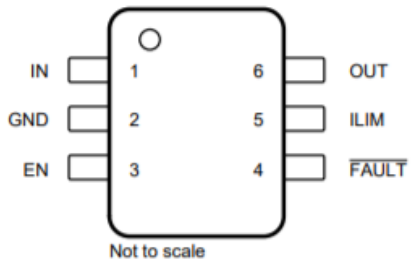
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS25221	SOT-23 (6)	2.90 mm x 1.60 mm
	WSON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

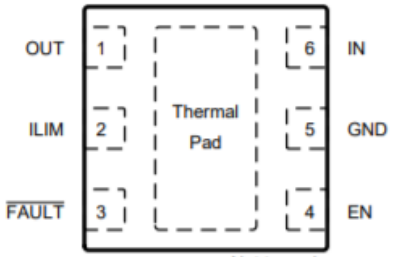
Pin Configuration and Functions

DBV PACKAGE
SOT-23 6-Pin
Top View



Not to scale

DRV PACKAGE
WSON 6-Pin
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	WSON		
IN	1	6	I	Input voltage and power switch drain; connect a 0.1 µF or greater ceramic capacitor from IN to GND close to IC
GND	2	5	--	Ground connection
EN	3	4	I	Enable input, logic high/low turns on power switch
$\overline{FAULT}$	4	3	O	Active-low open-drain output, asserted during over-current, or over-temperature conditions
ILIM	5	2	O	External resistor used to set current limit threshold
OUT	6	1	O	Power switch output, connect to load
Thermal Pad	--	PAD	--	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect thermal pad to GND pin externally.

7.5 Electrical Characteristics

over recommended operating conditions, $V_{EN} = V_{IN}$, R_{FAULT} = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	Static drain-source on-state resistance	DBV package, T_J = 25°C			70	80	mΩ
		DBV package, –40°C ≤T_J ≤125°C				110	
		DRV package, T_J = 25°C			70	92	
		DRV package, –40°C ≤T_J ≤125°C				122	
t_r	Rise time, output	V_{IN} = 5.5 V	C_L = 1 µF, R_L = 100 Ω, (see 図 1)		0.55	0.95	ms
		V_{IN} = 2.5 V			0.35	0.62	
t_f	Fall time, output	V_{IN} = 5.5 V			0.24	0.3	
		V_{IN} = 2.5 V			0.22	0.28	
ENABLE INPUT EN OR $\overline{EN}$							
	Enable pin turn on/off threshold			0.8		1.6	V
I_{EN}	Input current	V_{EN} = 0 V or 5.5 V		-0.5	0	0.5	µA
t_{on}	Turnon time	C_L = 1 µF, R_L = 100 Ω, (see 図 2)				3	ms
t_{off}	Turnoff time	C_L = 1 µF, R_L = 100 Ω, (see 図 2)				0.7	ms
CURRENT LIMIT							
I_{OS}	Current-limit threshold (Maximum DC output current I_{OUT} delivered to load) and Short-circuit current, OUT connected to GND	R_{ILIM} = 20 kΩ	T_J = 25°C	2585	2720	2850	mA
			–40°C ≤T_J ≤125°C	2560		2880	
		R_{ILIM} = 30 kΩ	T_J = 25°C	1710	1820	1930	
			–40°C ≤T_J ≤125°C	1700		1945	
		R_{ILIM} = 80 kΩ	T_J = 25°C	630	690	755	
			–40°C ≤T_J ≤125°C	610		790	
		R_{ILIM} = 210 kΩ	T_J = 25°C	220	275	330	
			–40°C ≤T_J ≤125°C	210		370	
t_{IOS}	Response time to short circuit	V_{IN} = 5 V (see 図 4)			1.5		µs
SUPPLY CURRENT							
I_{SD}	Supply current, switch disable	V_{IN} = 5.5 V, No load on OUT, V_{EN} = 0 V,R_{ILIM} = 20 kΩ			0.02	0.5	µA
I_{SE}	Supply current, switch enable	V_{IN} = 5.5 V, No load on OUT ,R_{ILIM} = 20 kΩ			75	90	µA
UNDERVOLTAGE LOCKOUT							
UVLO	Low-level input voltage, IN	V_{IN} rising			2.37	2.47	V
	Hysteresis, IN	T_J = 25 °C			45		mV
$\overline{FAULT}$ FLAG							
V_{OL}	Output low voltage, $\overline{FAULT}$	$I_{/FAULT}$ = 1 mA				180	mV
	Off-state leakage	$V_{/FAULT}$ = 5.5 V				0.5	µA
	$\overline{FAULT}$ deglitch	$\overline{FAULT}$ assertion or de-assertion due to overcurrent condition		6	8	12	ms
THERMAL SHUTDOWN							
	Thermal shutdown threshold				165		°C
	Thermal shutdown threshold in current-limit				145		°C
	Hysteresis				20		°C

10. CI INTERFACE

17MB171 Digital CI ve Smart Card Interface Block diagram:

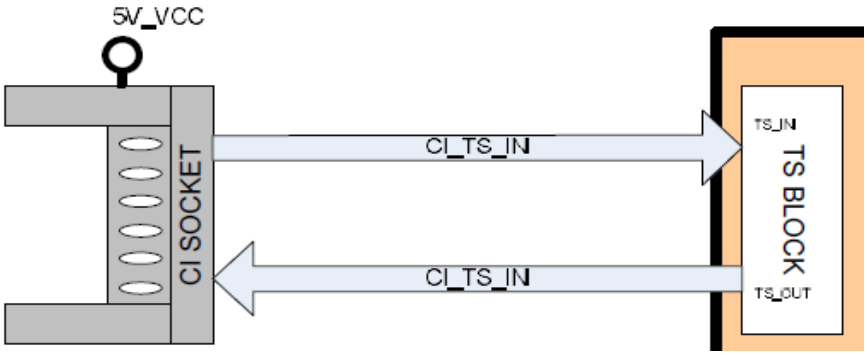


Figure 12: CI interface

11. SOFTWARE UPDATE

MAIN SOFTWARE UPDATE

In MB171 project, please follow software update procedure:

Method-1

1. Copy MstarUpgrade.bin to USB stick (root directory, FAT32)
2. Enter M-Boot console first (Long press "ENTER" key on Tera Term Console when your device reboot then do AC On)
3. Plug the USB stick to your target board
4. Execute "custar" in M-Boot console to perform upgrading

Method-2

1. Copy upgrade_loader.pkg to root folder of USB stick (or copy upgrade_loader_no_tvcertificate.pkg if you don't want to erase keys, credentials, etc.)
2. Insert USB disk to one of the USB ports on your TV
3. Power on TV and wait until you see the bootlogo
4. You should see logs like below

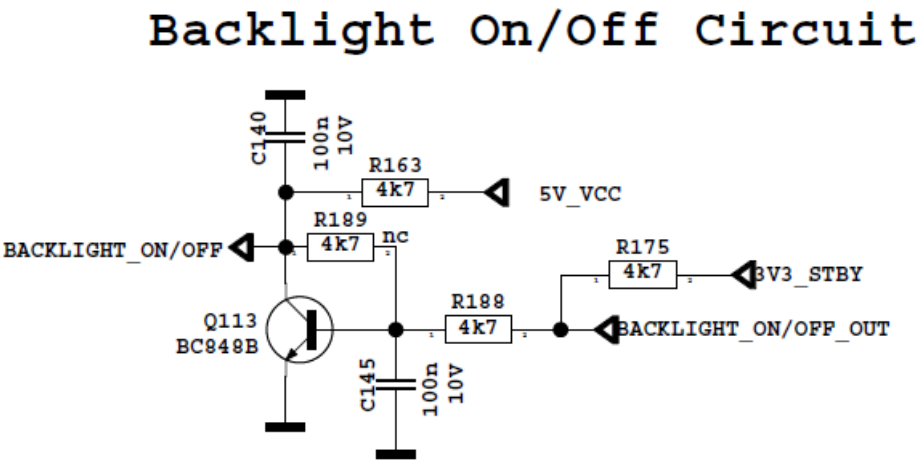
12. TROUBLESHOOTING

A. NO BACKLIGHT PROBLEM

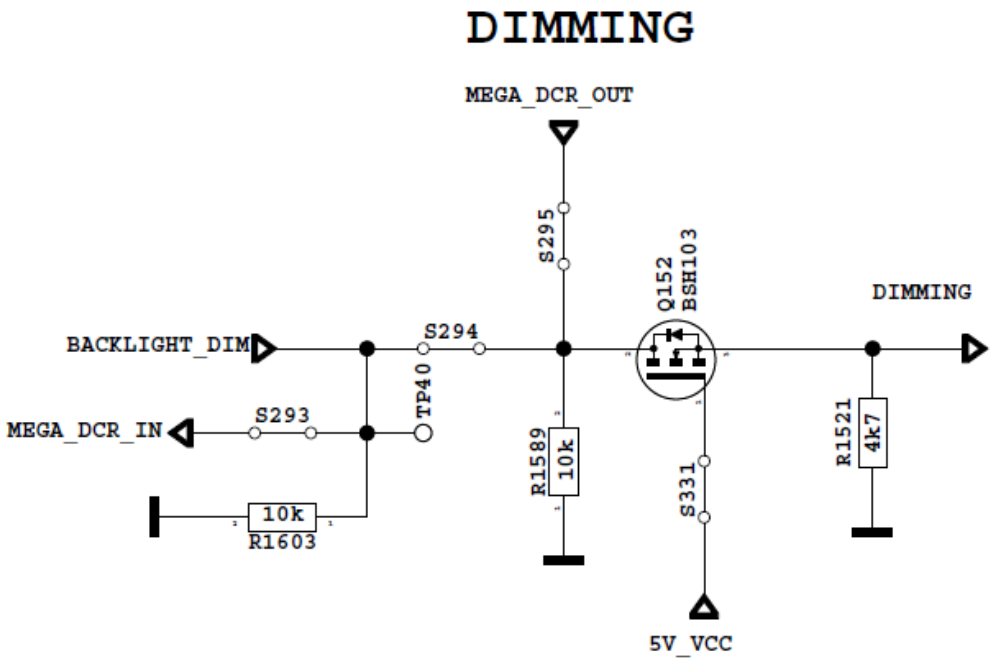
Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply, stby on/off pin

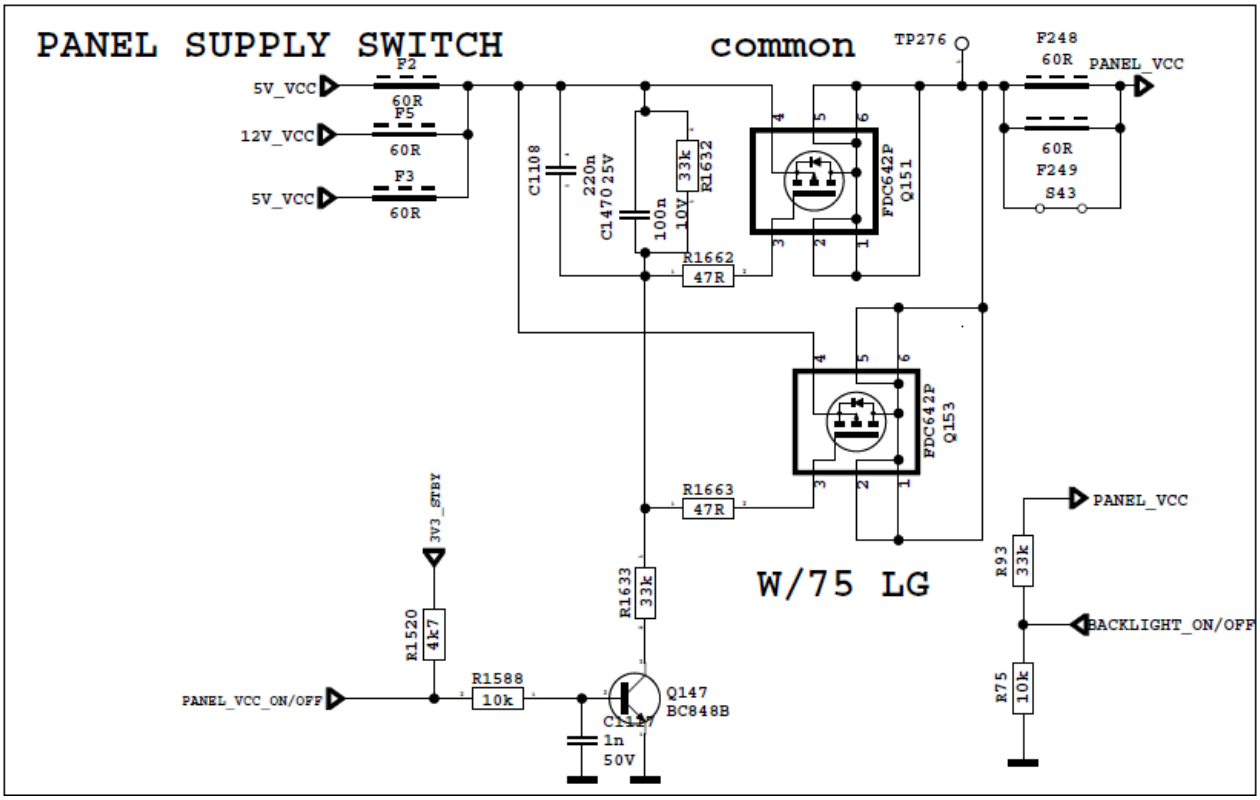
BACKLIGHT_ON/OFF pin should be high when the backlight is ON. Collector pin of Q113 must be low when the backlight is OFF. If it is a problem, please check Q181. Also it can be tested in TP500 or Pin5 of CN2 in main board. Please also check panel cables.



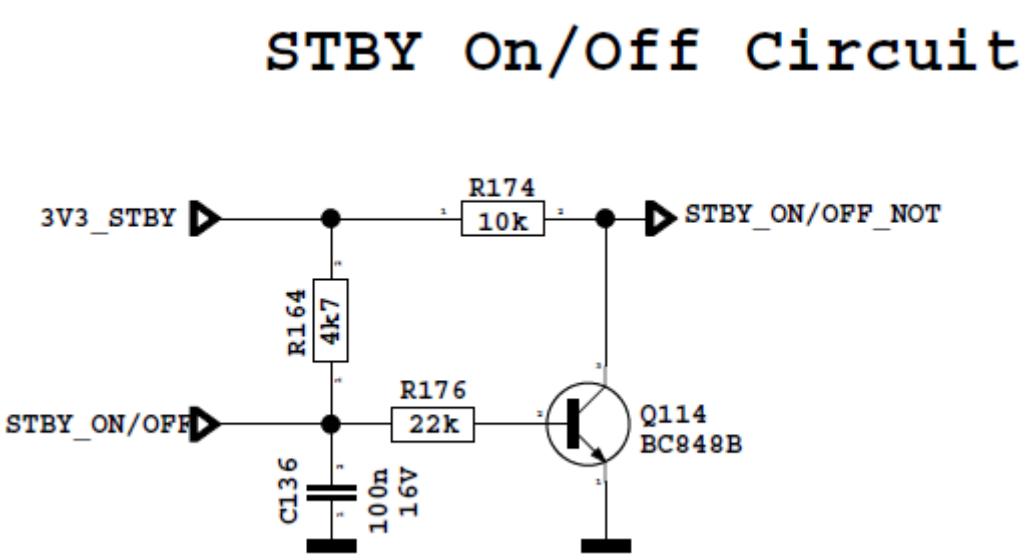
Dimming pin should be high or square wave in open position. If it is low, please check S294 for MTK side. It also can be checked at TP499. Please also check panel or power cables and connectors.



Panel power supply should be in panel specs. Please check Q151, shown below; also it can be checked TP276.



STBY_ON/OFF should be low for TV on condition, please check Q114's collector.

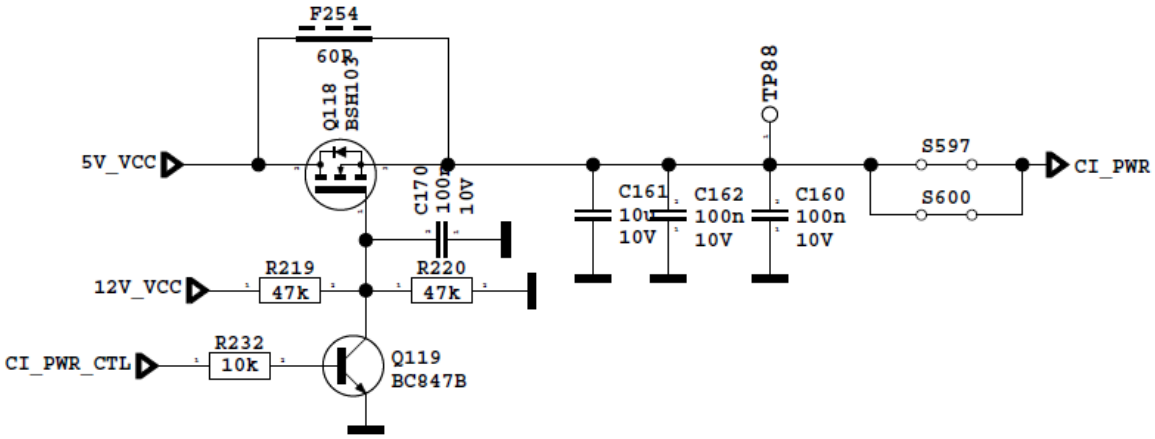


B. CI MODULE PROBLEM

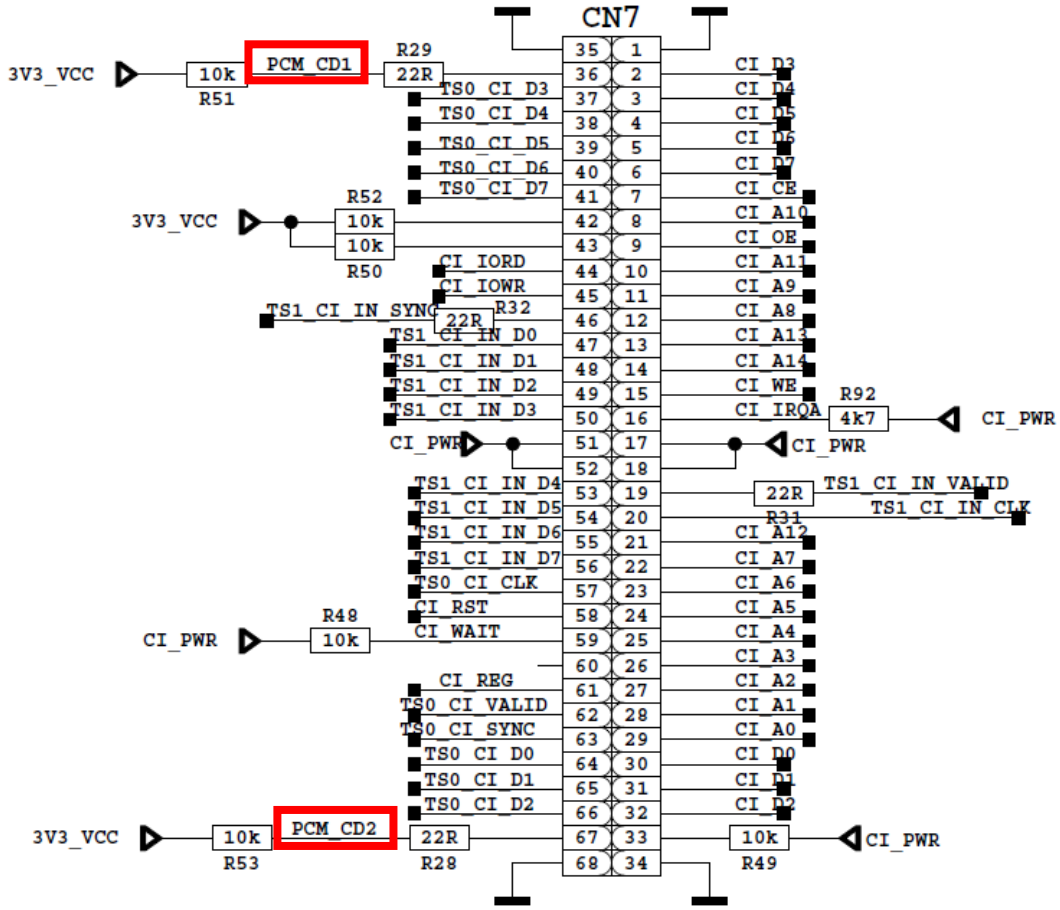
Problem: CI is not working when CI module inserted.

Possible causes: Supply, supply control pin, detects pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTRL, this pin should be low.



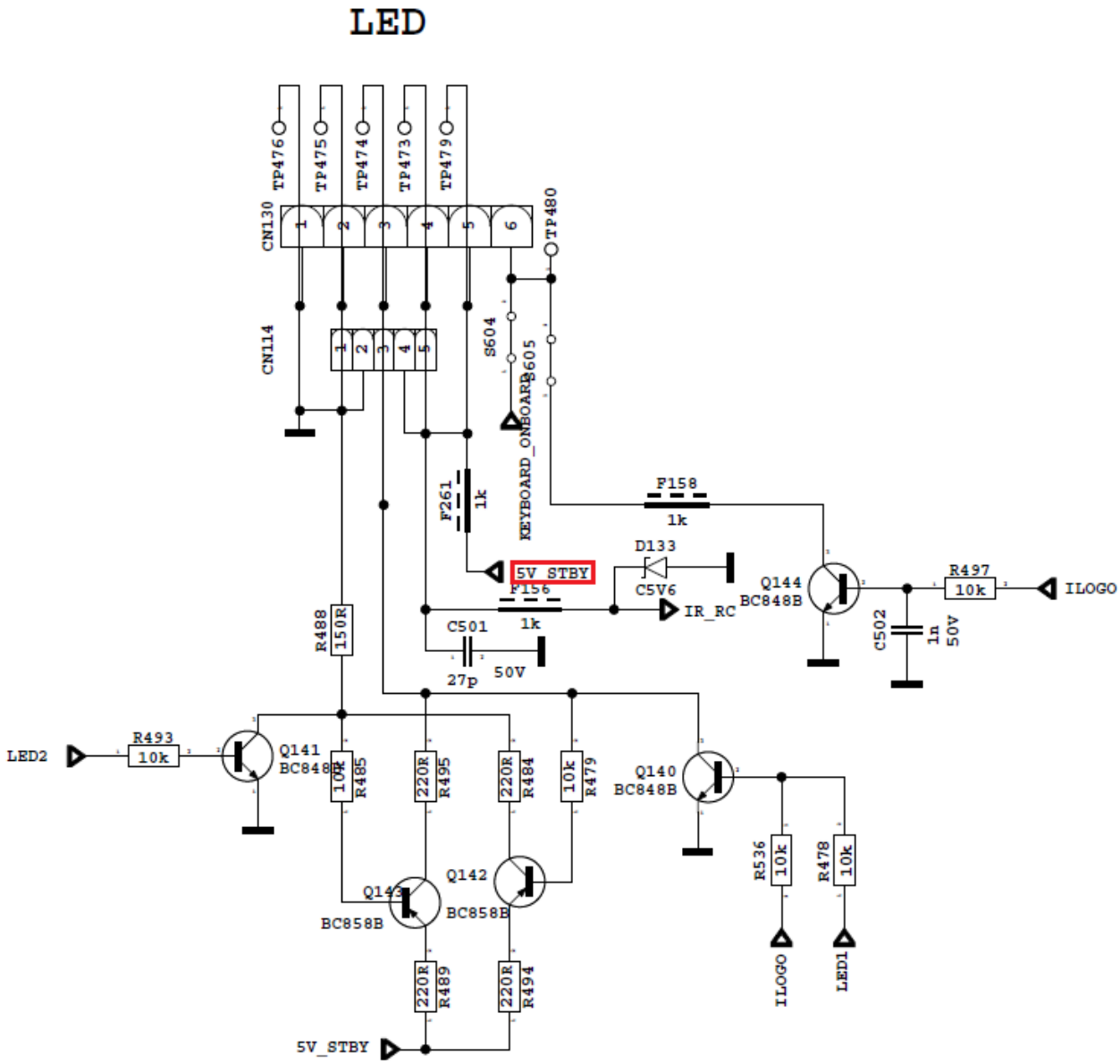
- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.


CN7
3V3_VCC
10k
R51
PCM_CD1
R29
22R
TS0_CI_D3
TS0_CI_D4
TS0_CI_D5
TS0_CI_D6
TS0_CI_D7
R52
10k
10k
R50
CI_IORD
CI_IOWR
TS1_CI_IN_SYNC
R32
22R
TS1_CI_IN_D0
TS1_CI_IN_D1
TS1_CI_IN_D2
TS1_CI_IN_D3
CI_PWR
TS1_CI_IN_D4
TS1_CI_IN_D5
TS1_CI_IN_D6
TS1_CI_IN_D7
TS0_CI_CLK
CI_RST
CI_WAIT
R48
10k
CI_REG
TS0_CI_VALID
TS0_CI_SYNC
TS0_CI_D0
TS0_CI_D1
TS0_CI_D2
3V3_VCC
10k
R53
PCM_CD2
22R
R28
CI_D3
CI_D4
CI_D5
CI_D6
CI_D7
CI_CE
CI_A10
CI_OE
CI_A11
CI_A9
CI_A8
CI_A13
CI_A14
CI_WE
CI_IRQA
R92
4k7
CI_PWR
CI_PWR
22R
TS1_CI_IN_VALID
TS1_CI_IN_CLK
R31
CI_A12
CI_A7
CI_A6
CI_A5
CI_A4
CI_A3
CI_A2
CI_A1
CI_A0
CI_D0
CI_D1
CI_D2
10k
R49
CI_PWR

C. IR PROBLEM

Problem: LED or IR not working

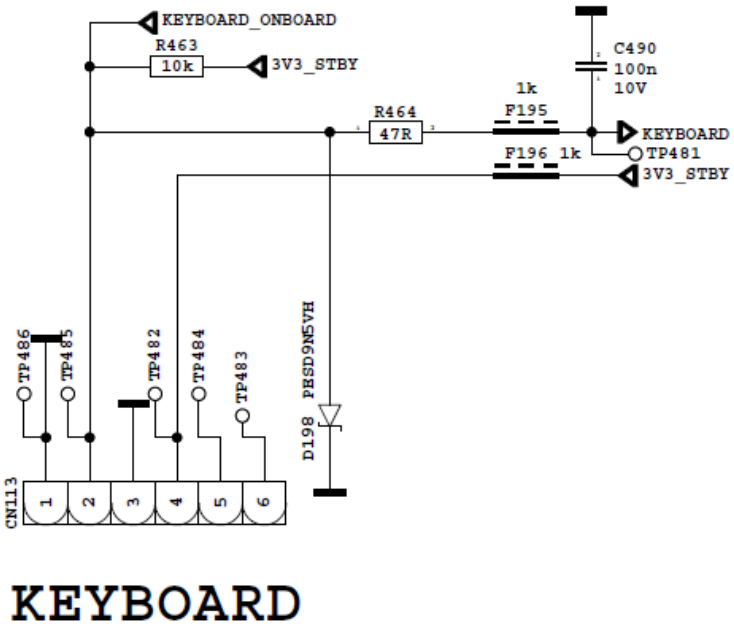
Check LED card supply on MB170 chasis.



D. KEYPAD TOUCHPAD PROBLEMS

Problem: Keypad or Touchpad is not working

Check keypad supply on MB170.



E. USB PROBLEMS

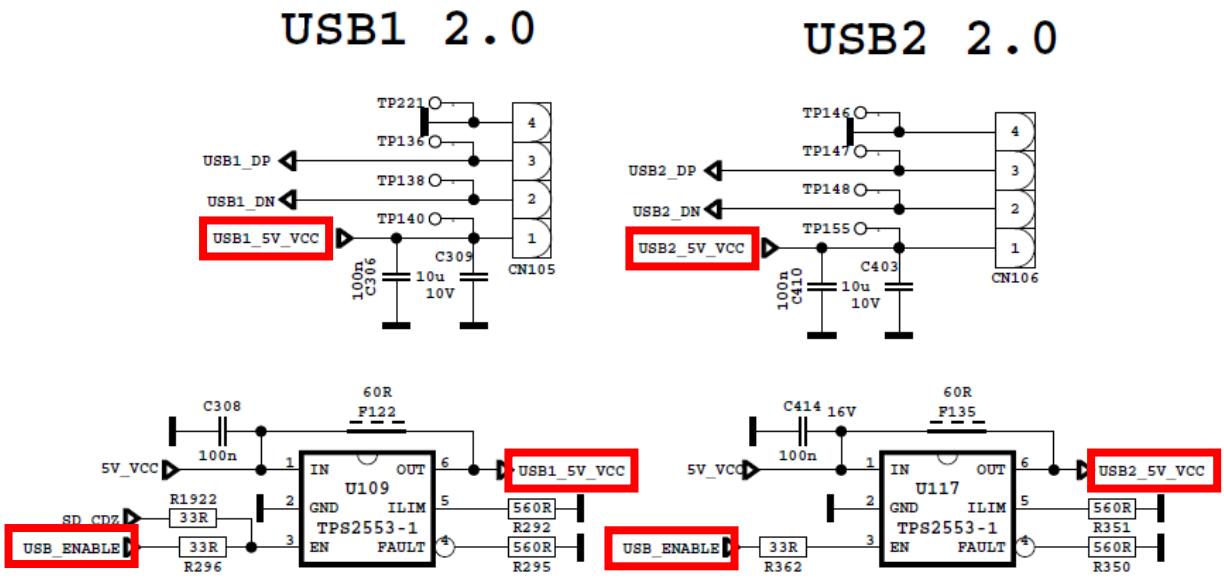
Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

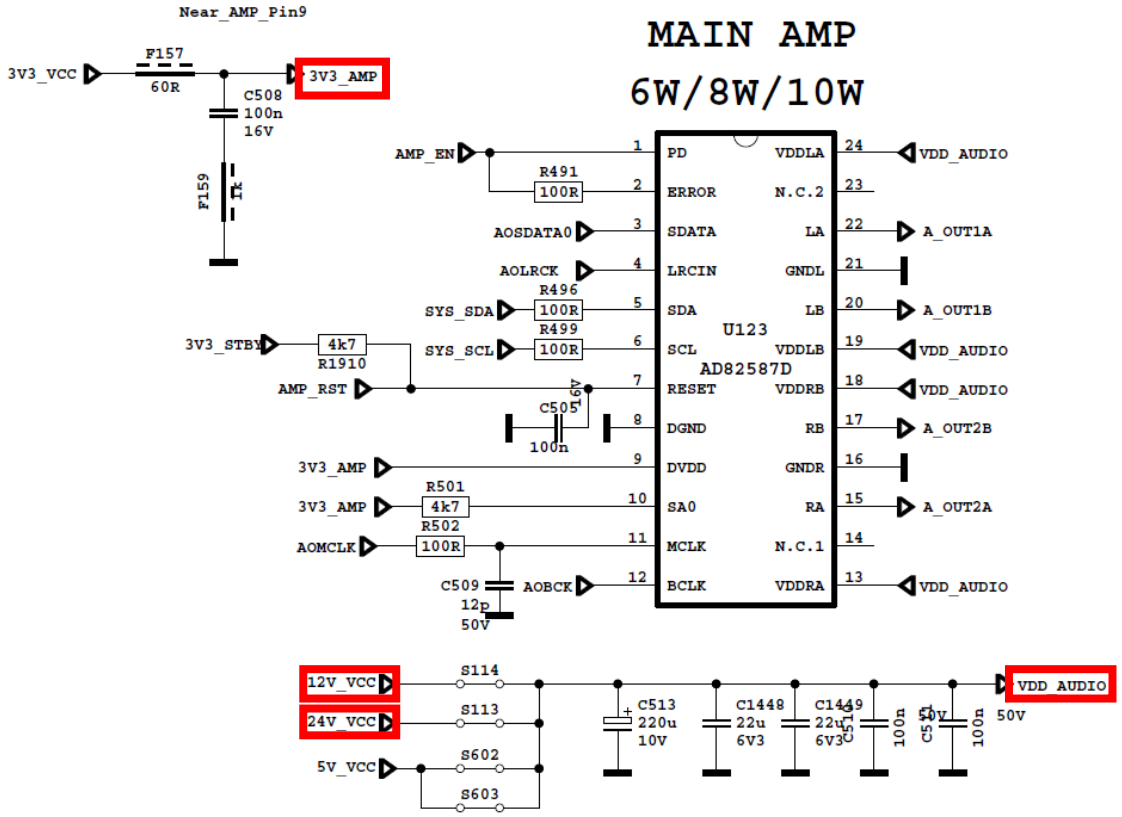
USB Control is optional, so U109 and U117 may not be added. Check supply voltages only.

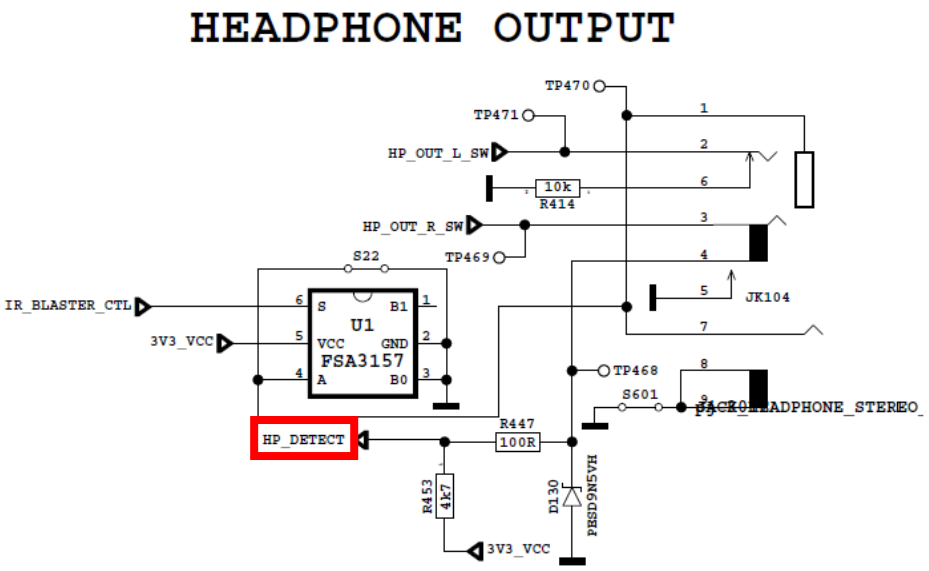


F. NO SOUND PROBLEM

Problem: No audio at main TV speaker outputs.

Check supply voltages of 24V_VCC, VDD_AUDIO and 3V3_AMP with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3V.





G. STANDBY ON/OFF PROBLEM

Problem: Device cannot boot, TV hangs in standby mode.

There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm program. These printouts may give a clue about the problem. You can use VGA for Teraterm program connection.

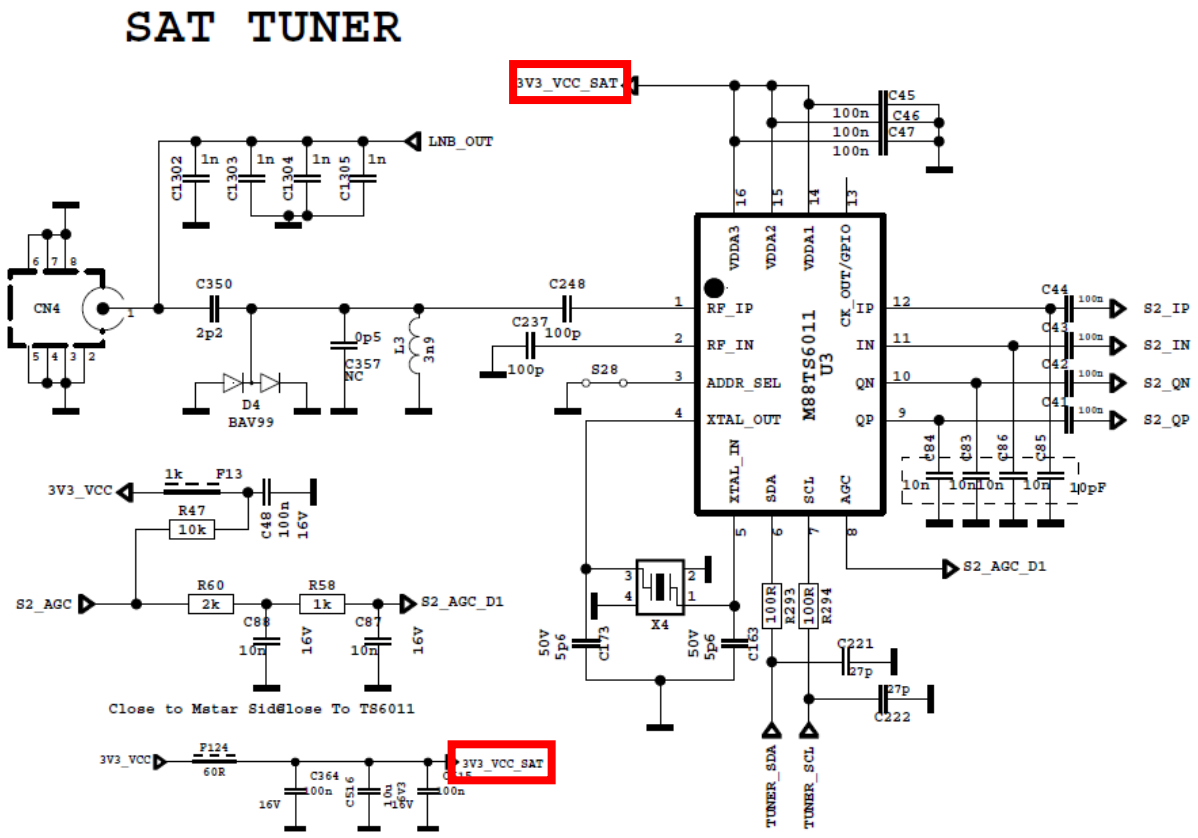
H. NO SIGNAL PROBLEM IN DVB-S/S2 MODE

Problem: No signal or Low signal in DVB-S/S2 mode.

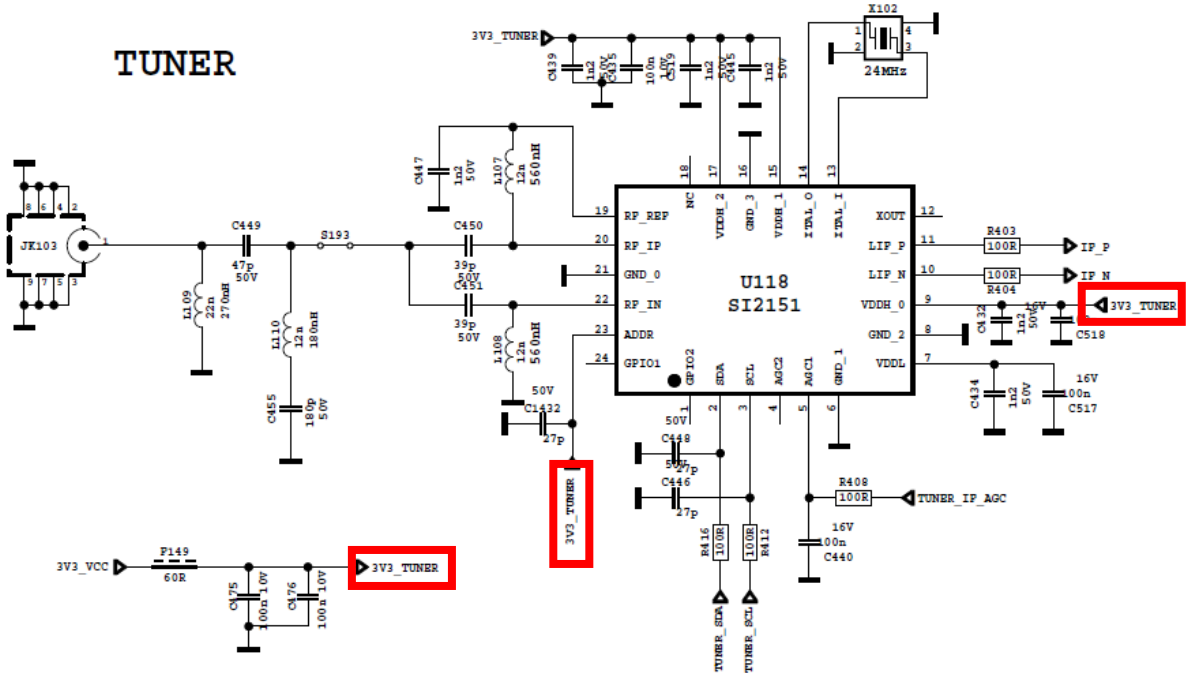
Check signal cables and LNB voltage, if there is no problem, check M88TS6011 (U3) supply voltages; 3V3_VCC_SAT.

If the above measurements are OK, then measure the voltage from the PIN1 of U3.

If the PIN9 voltage is equal to 0V, please check i2c waveforms and software. If the PIN9 voltage is lower than 1V(e.g: 0.8Vor 0.3V), change the U3 with a new part.



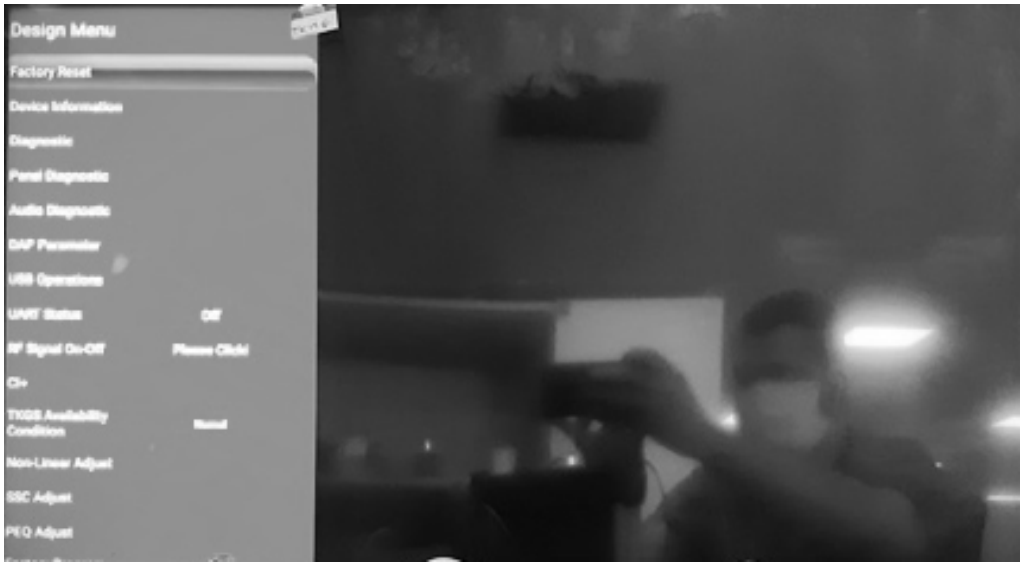
I. NO SIGNAL PROBLEM IN DVB-T MODE



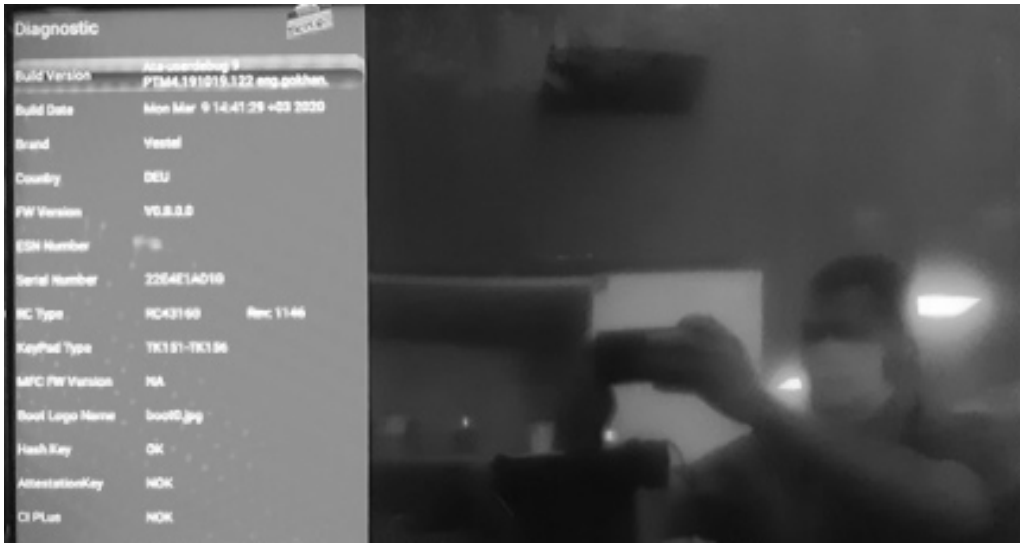
13. SERVICE MENU SETTINGS

In order to reach service menu, first chose Channel, then press **"MENU"** buton, press **"Advanced Options"** then write "**4725"** by using remote controller.

You can see the service menu main screen below. You can check SW releases by using this menu under Diagnostic title. In addition, you can make changes on video settings, audio settings, DAP Parameters etc. using regarding titles. You may also use USB Operations for SW update and update Unique Keys and Configuration files.

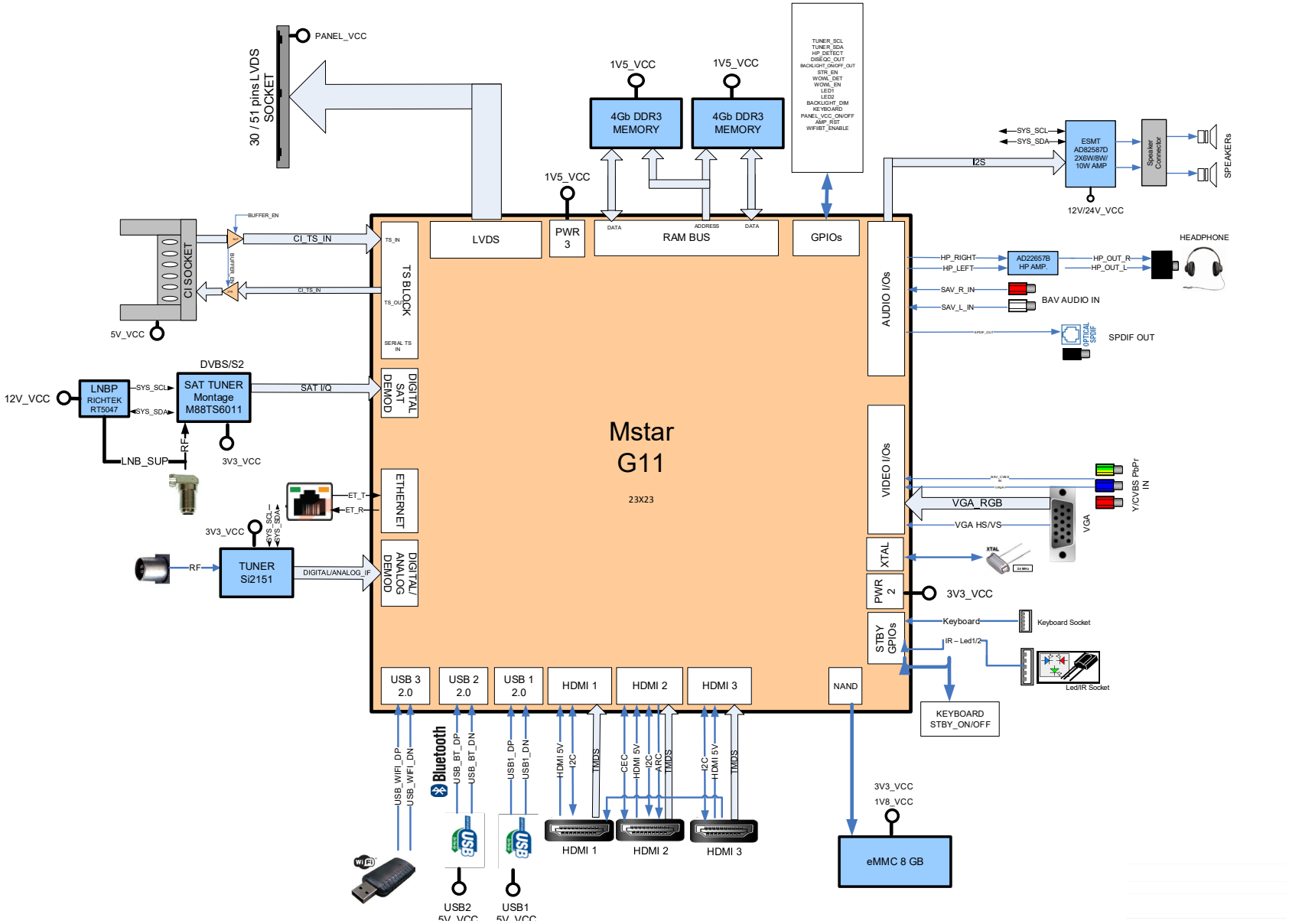


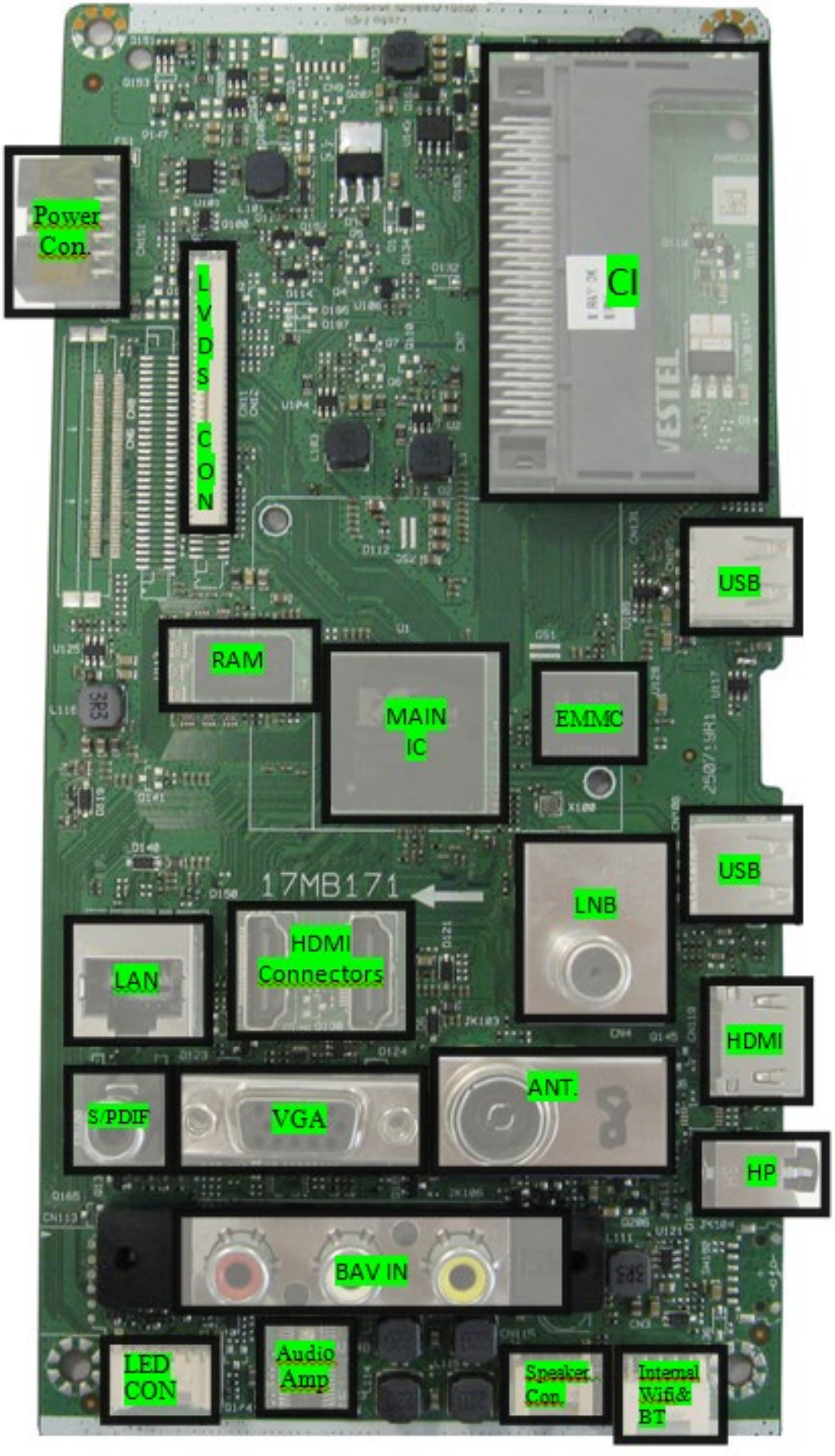
Service Menu

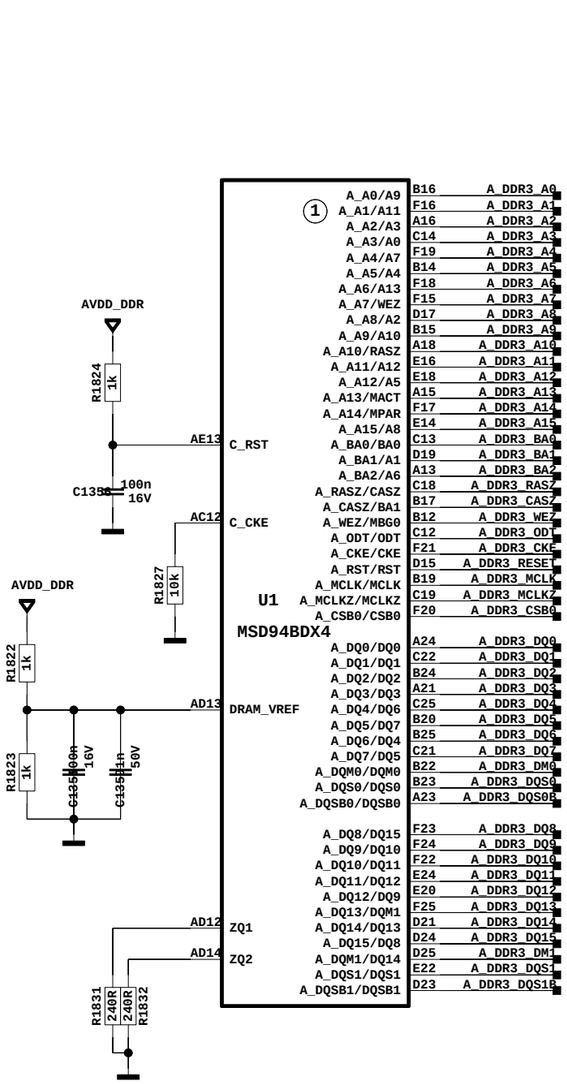


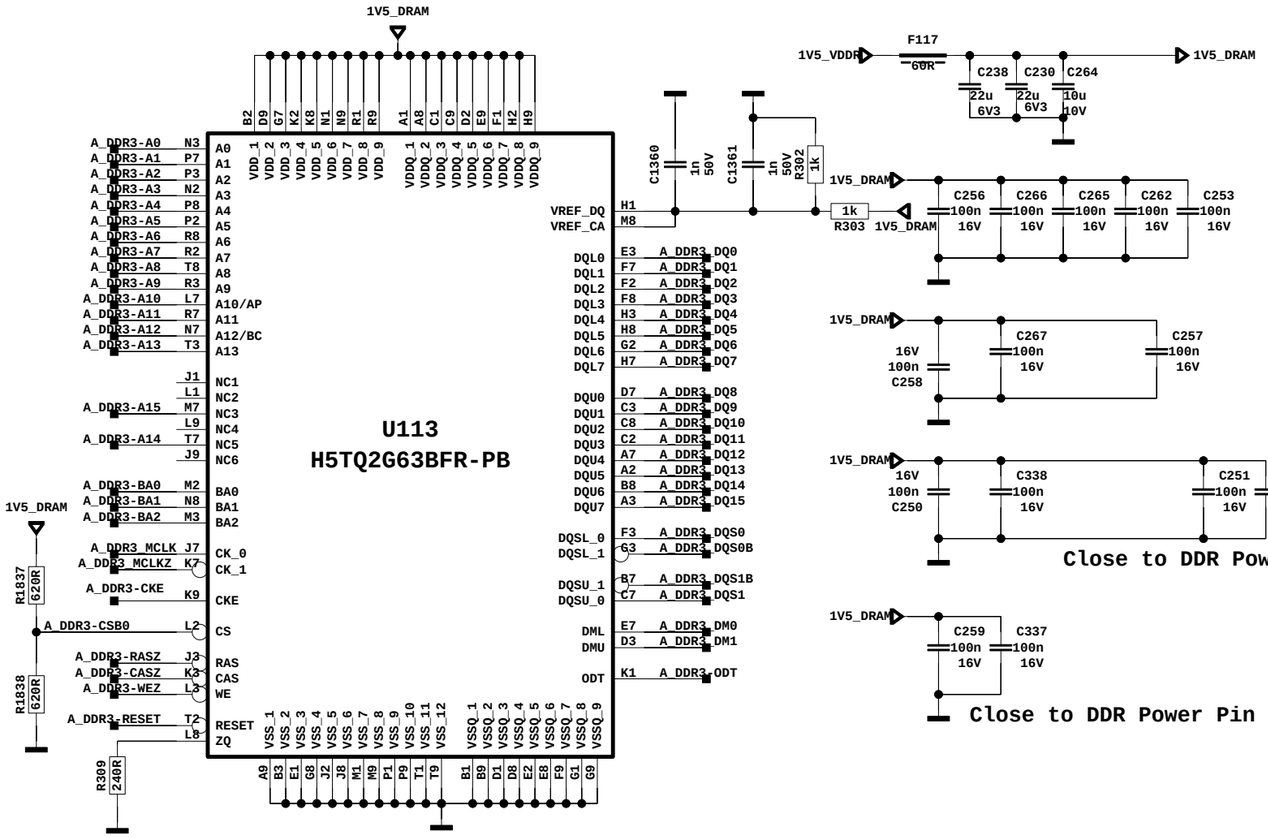
Diagnostic

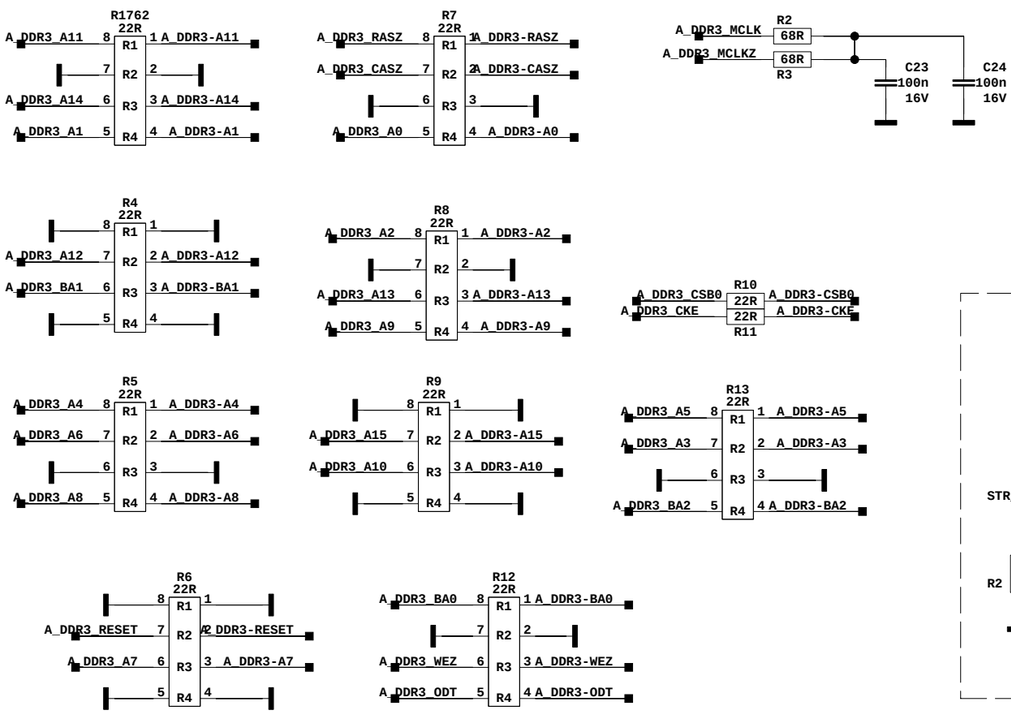
14. GENERAL BLOCK DIAGRAM

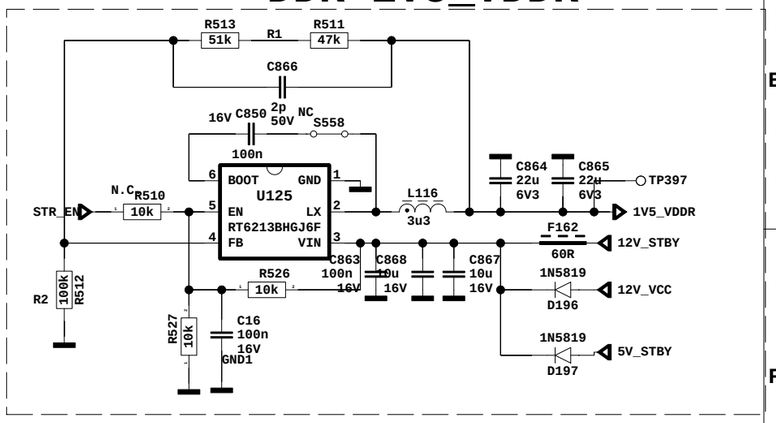



Power Con.
LVDS CON
CI
USB
RAM
MAIN IC
EMMC
USB
17MB171
LNB
LAN
HDMI Connectors
HDMI
S/PDIF
VGA
ANT.
HP
BAV IN
LED CON
Audio Amp
Speaker Con.
Internal Wifi& BT

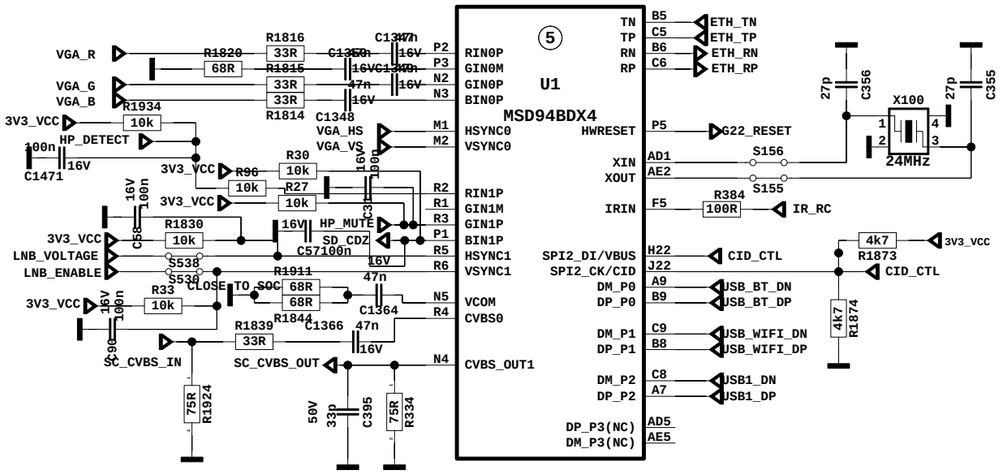


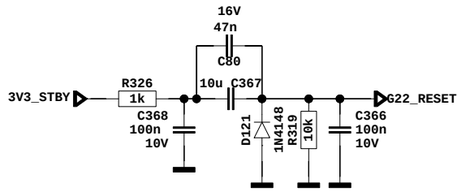


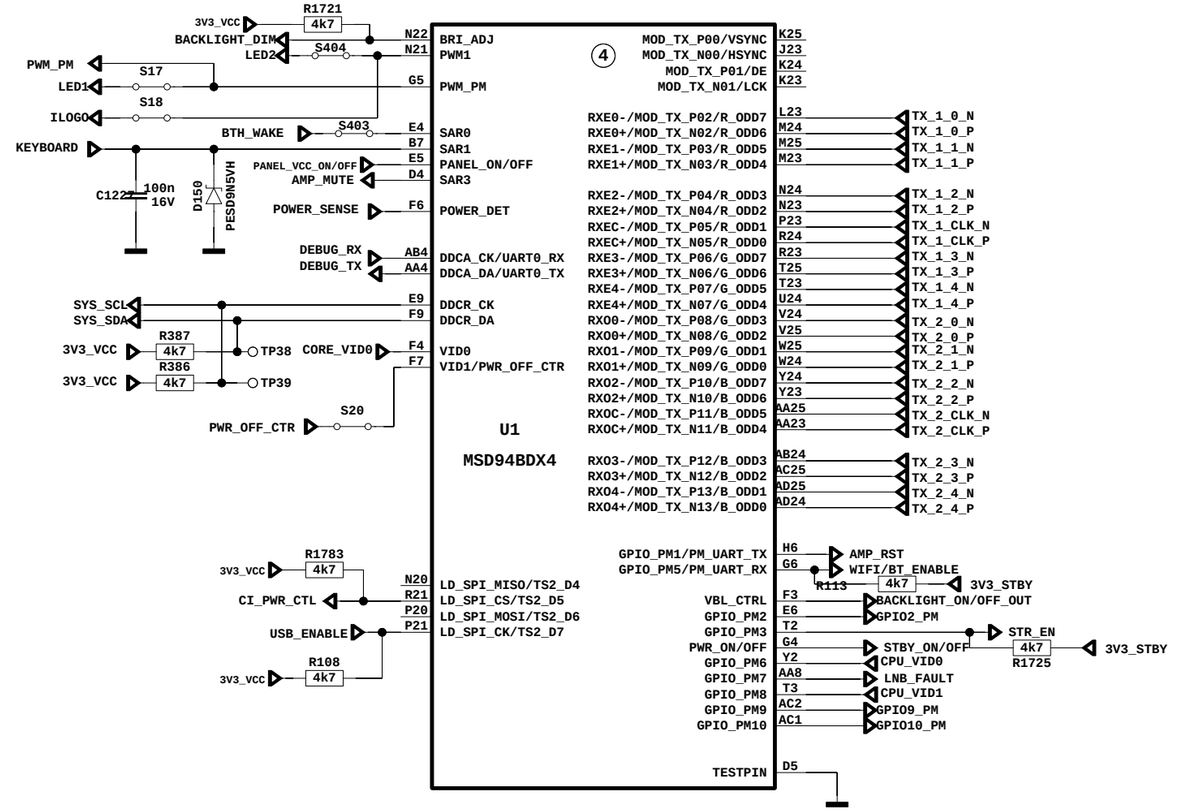


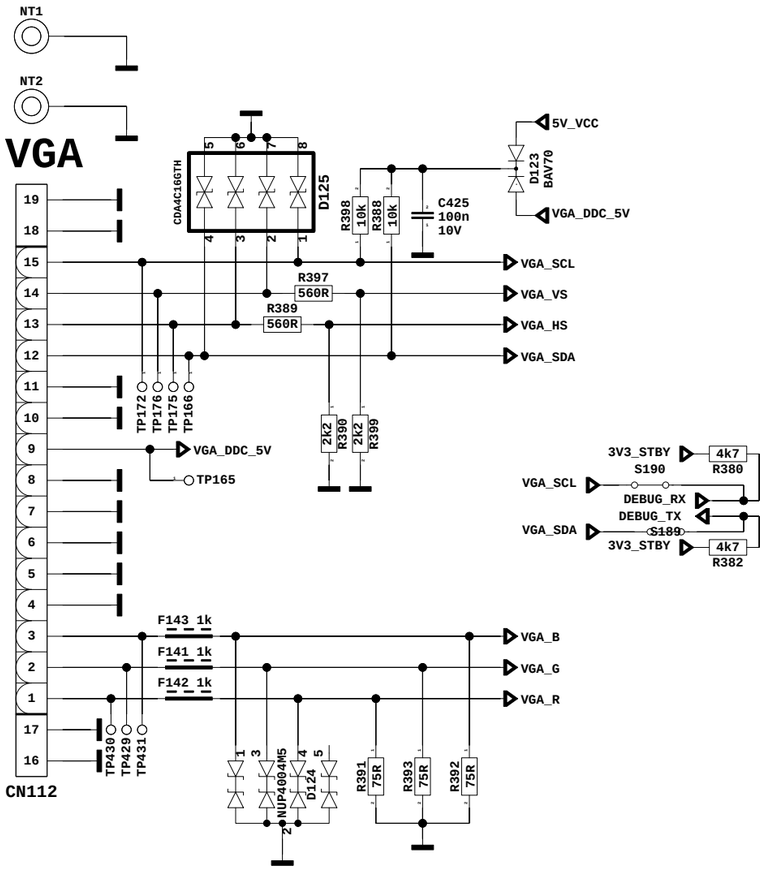


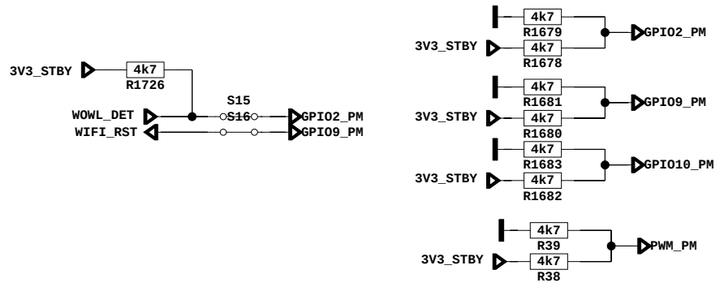
VESTEL	PROJECT NAME : 17mb171-r2a	A3
SCH NAME :DDR		T. SHT 11
DRAWN BY :<YOUR NAME HERE>		25/12/2019:13:58

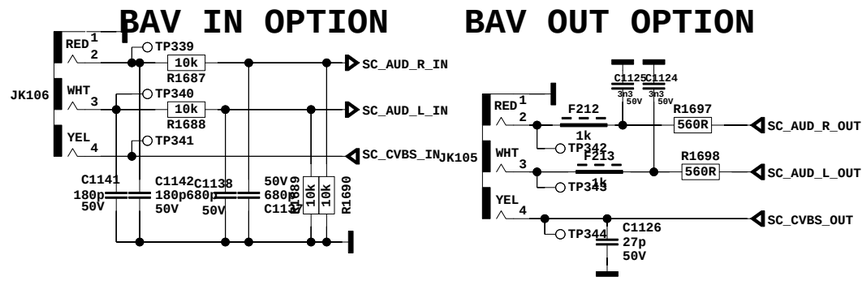


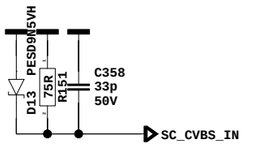












VESTEL	PROJECT NAME : 17mb171-r2a	A3
SCH NAME :PERIPHERALS_GPIO	T. SHT	11
DRAWN BY :<YOUR NAME HERE>	25/12/2019:13:58	

HDMI1 (SIDE)

CN119

HDMI0_RX2P
HDMI0_RX2N
HDMI0_RX1P
HDMI0_RX1N
HDMI0_RX0P
HDMI0_RX0N
HDMI0_CLKP
HDMI0_CLKN
CEC
HDMI0_SCL
HDMI0_SDA
HDMI0_5V
TP33
TP32
TP31
R538 47k
R537 47k
1k R539
S531
10k R534
HOTPLUG0
R535 10k
Q145 BC848B

HDMI0_RX0N J1
HDMI0_RX0P J2
HDMI0_RX1N K3
HDMI0_RX1P K2
HDMI0_RX2N L3
HDMI0_RX2P L2
HDMI0_CLKN H1
HDMI0_CLKP J3
HDMI0_SCL L5
HDMI0_SDA M5
HOTPLUG0 M6
N6
6V3 1u C70
CEC R352 100R
P6

HDMI2_RX0N E2
HDMI2_RX0P F1
HDMI2_RX1N F2
HDMI2_RX1P G3
HDMI2_RX2N G2
HDMI2_RX2P H3
HDMI2_CLKN D3
HDMI2_CLKP E1
HDMI2_SCL K4
HDMI2_SDA K5
HOTPLUG2 L6
M4
C71 1u 6V3

HDMI1_RX0N B3
HDMI1_RX0P B2
HDMI1_RX1N B1
HDMI1_RX1P C2
HDMI1_RX2N C1
HDMI1_RX2P D2
HDMI1_CLKN A3
HDMI1_CLKP A2
HDMI1_SCL J5
HDMI1_SDA H5
HOTPLUG1 J6
K6
C72 1u 6V3

HDMI1_5V R77 10k
33k R105
E10
SPDIF_OUT D10

RX0N
RX0P
RX1N
RX1P
RX2N
RX2P
RXCN
RXCP
DDCDA_CK
DDCDA_DA
HOTPLUGA
NODIE/PAD_HOTPLUGA_HDMI20_5V
CEC0

B_RX0N
B_RX0P
B_RX1N
B_RX1P
B_RX2N
B_RX2P
B_RXCN
B_RXCP
DDCDB_CK
DDCDB_DA
HOTPLUGB
DVDD_NODIE/PAD_HOTPLUGB_HDMI20_5V

C_RX0N
C_RX0P
C_RX1N
C_RX1P
C_RX2N
C_RX2P
C_RXCN
C_RXCP
DDCDC_CK
DDCDC_DA
HOTPLUGC
DVDD_NODIE/PAD_HOTPLUGC_HDMI20_5V

SPDIF_IN
SPDIF_OUT

U1
MSD94BDX4

LINEIN_L0 V2
LINEIN_R0 V3
LINEIN_L4 W2
LINEIN_R4 W3
LINEOUT_L0 AA5
LINEOUT_R0 AA6
LINEOUT_L2 Y6
LINEOUT_R2 Y5
EARPHONE_OUTL AB5
EARPHONE_OUTR AB6
ARC0 J4
AUVAG V1
AUVRM U3
I2S_OUT_BCK D9
I2S_OUT_MCK F8
I2S_OUT_SD E8
I2S_OUT_WS D8

C61 4u7 6V3
C301 4u7 6V3
SC_AUD_L_IN
SC_AUD_R_IN
50V C63 100n C62 100n C65 100n C64
3n3 3n3 3n3 3n3
S36 S38 S37 S35
SC_DAC_L
SC_DAC_R
HP_LEFT
HP_RIGHT
S34 C59 1u 6V3
HDMI_ARC
C604u7 C30 100n 16V
F9 220R
R40 4k7
R41 4k7
R14 22R
12p 50V C66 C67 12p
AOMCLK
AOBCK
AOSDATA0
AOLRCK

HDMI3

CN109

HDMI1_RX2P
HDMI1_RX2N
HDMI1_RX1P
HDMI1_RX1N
HDMI1_RX0P
HDMI1_RX0N
HDMI1_CLKP
HDMI1_CLKN
CEC
HDMI_ARC
HDMI1_SCL
HDMI1_SDA
TP34
TP35
TP36
HDMI1_5V
1k R369
HDMI1_5V
R359 47k
R358 47k
S532
10k R368
R376 10k
Q131 BC848B
HOTPLUG1

HDMI2

CN5

HDMI2_RX2P
HDMI2_RX2N
HDMI2_RX1P
HDMI2_RX1N
HDMI2_RX0P
HDMI2_RX0N
HDMI2_CLKP
HDMI2_CLKN
CEC
TP37
HDMI2_SCL
HDMI2_SDA
TP41
HDMI2_5V
TP42
1k R366
HDMI2_5V
R356 47k
R357 47k
S533
10k R365
R374 10k
Q130 BC848B
HOTPLUG2

S151 330ohms

USB1 2.0

TP221
TP136
TP138
TP140
USB1_DP
USB1_DN
USB1_5V_VCC
C309 10u 10V
100n C306
CN105

C308 100n
60R F122
5V_VCC
IN OUT
U109
GND ILIM
TPS2553-1
EN FAULT
USB1_5V_VCC
USB_ENABLE
33R R296
560R R292
560R R295

USB2 2.0

TP146
TP147
TP148
TP155
USB2_DP
USB2_DN
USB2_5V_VCC
C403 10u 10V
100n C410
CN106

C414 100n 16V
60R F135
5V_VCC
IN OUT
U117
GND ILIM
TPS2553-1
EN FAULT
USB2_5V_VCC
SD_CDZ
33R R362
560R R351
560R R350
R1 4k7

DAA INTERFACE

CN9

TP504
TP505
TP506
TP507
DAA_USB_DP
DAA_USB_DN
DAA_SPDIF
5V_DAA
S593
KEYBOARD_ONBOARD

DAA_USB_DP S584 DAA_USB_DP1
DAA_USB_DN S583 DAA_USB_DN1

SPDIF_COAX
S21
BSH103 Q202
DAA_SPDIF
R1888 4k7
R1889 4k7
R1887 4k7

5V_VCC
60R F251
C1431 10u 16V
100n C1426 16V
5V_DAA

ETHERNET

CN1

ETH_TP 1 TD+
5V_STBY F45 220R 1u C277
ETH_TN 2 TD-
3 TCT
ETH_RP 4 RD+
5V_STBY F46 120R C278
ETH_RN 5 RD-
6 RCT
IR_FROM_ETH 7 NC1
S432 8 NC2
9 SHLD1
10 SHLD2

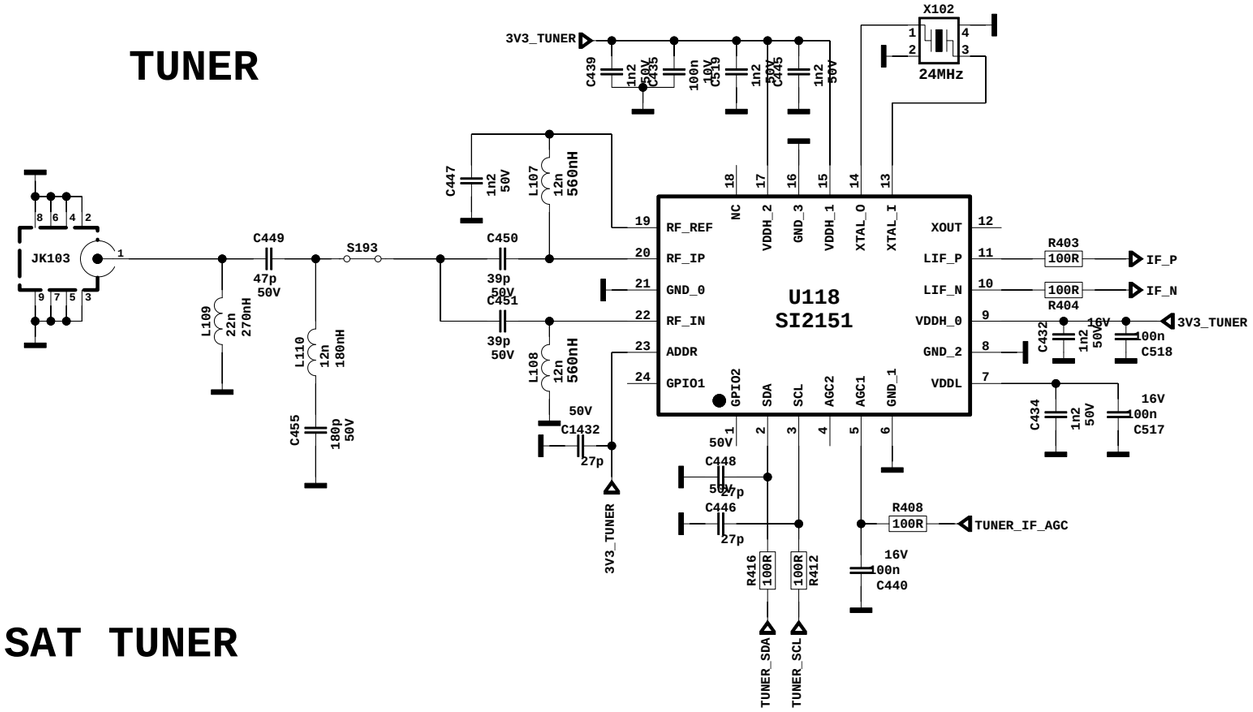
IR_FROM_ETH R270 100R
BC848B Q165
IR_RC
R267 100R 5V_STBY

ETH_TP S430 DEBUG_RX
ETH_TN S431 DEBUG_TX

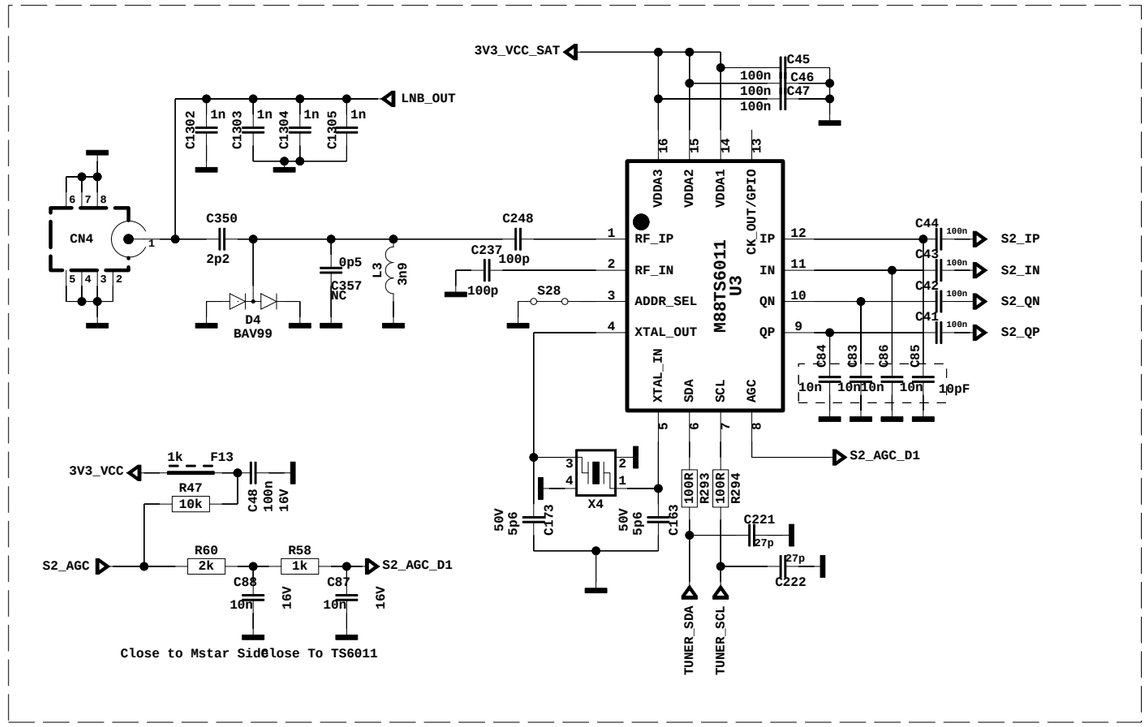
USB_BT_DP S409 USB_BT_DP2
USB_BT_DN S408 USB_BT_DN2
USB_BT_DP2 S7 USB2_DP
USB_BT_DN2 S6 USB2_DN
DAA_USB_DP1 S9 USB_BT_DP2
DAA_USB_DN1 S8 USB_BT_DN2

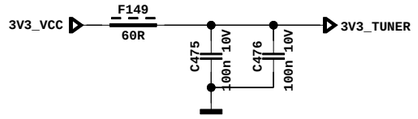
VESTEL	PROJECT NAME : 17mb171-r2a	A3
	SCH NAME : HDMI_USB_ETH	T. SHT 11
	DRAWN BY :<YOUR NAME HERE>	25/12/2019:13:58

TUNER

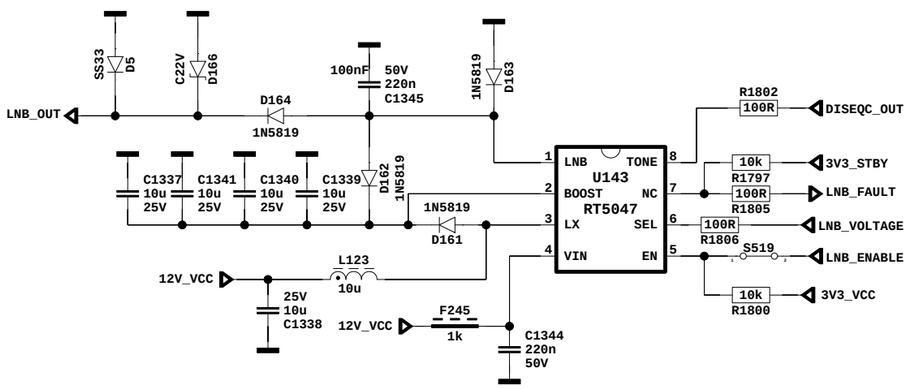


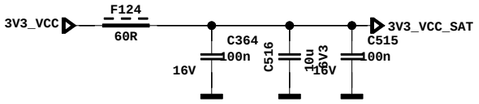
SAT TUNER



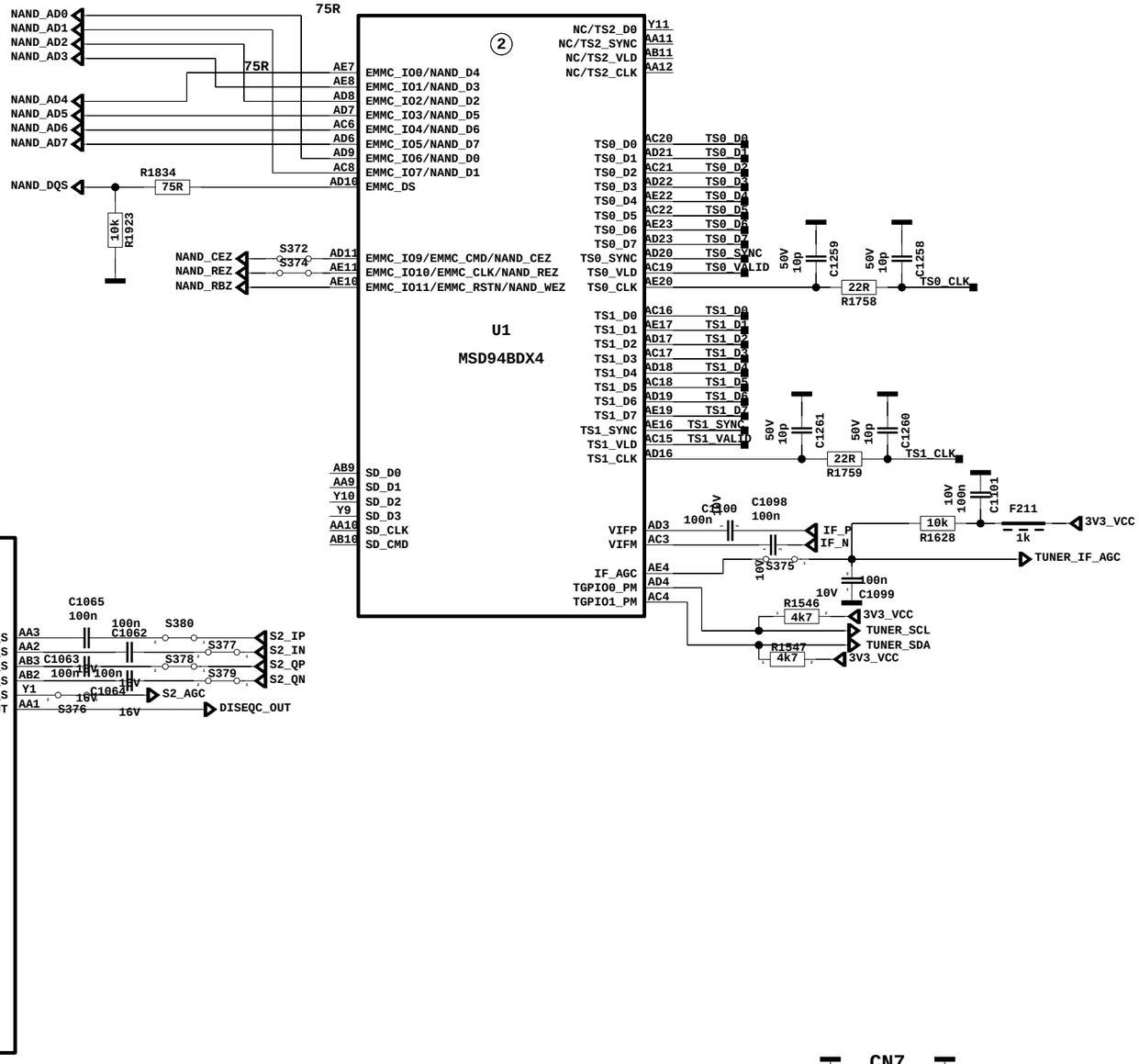


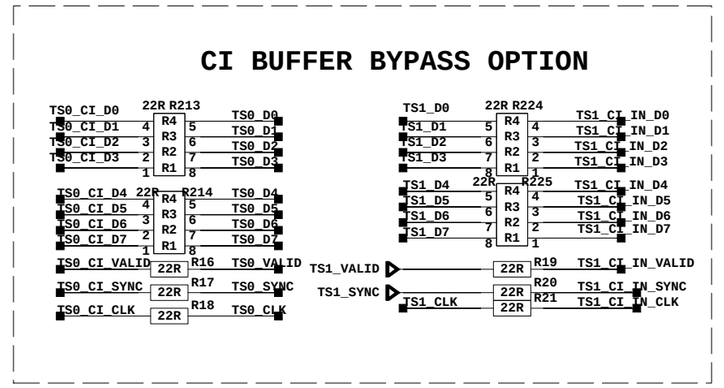
LNBp

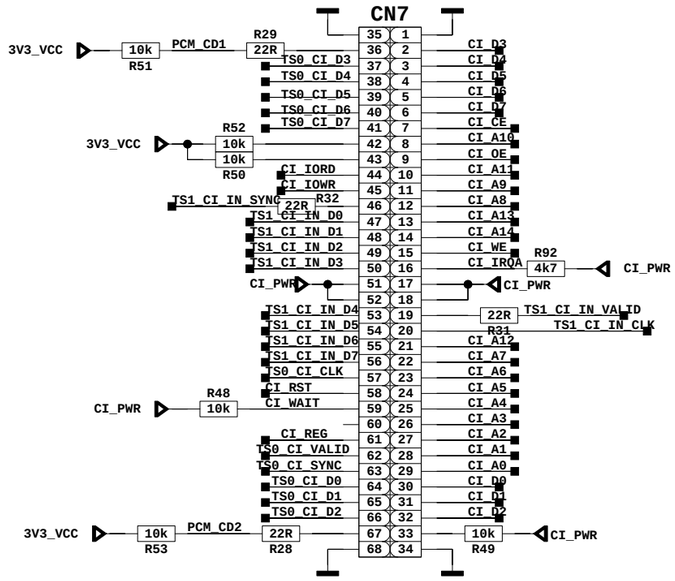


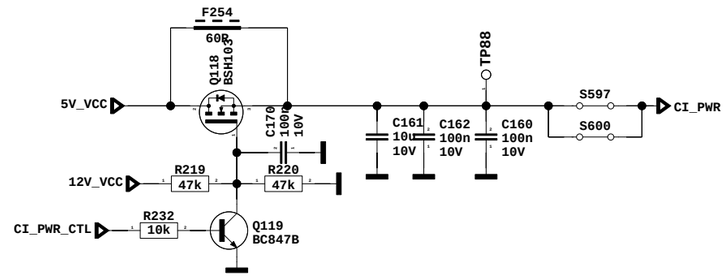


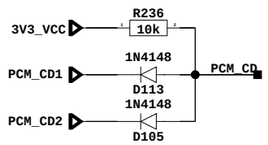
VESTEL	PROJECT NAME : 17mb171-r2a	A3
SCH NAME :TUNER_SAT_LNB		T. SHT 11
DRAWN BY :<YOUR NAME HERE>		25/12/2019:13:58

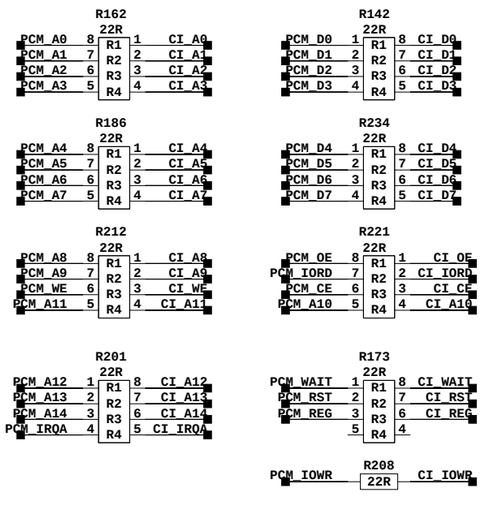






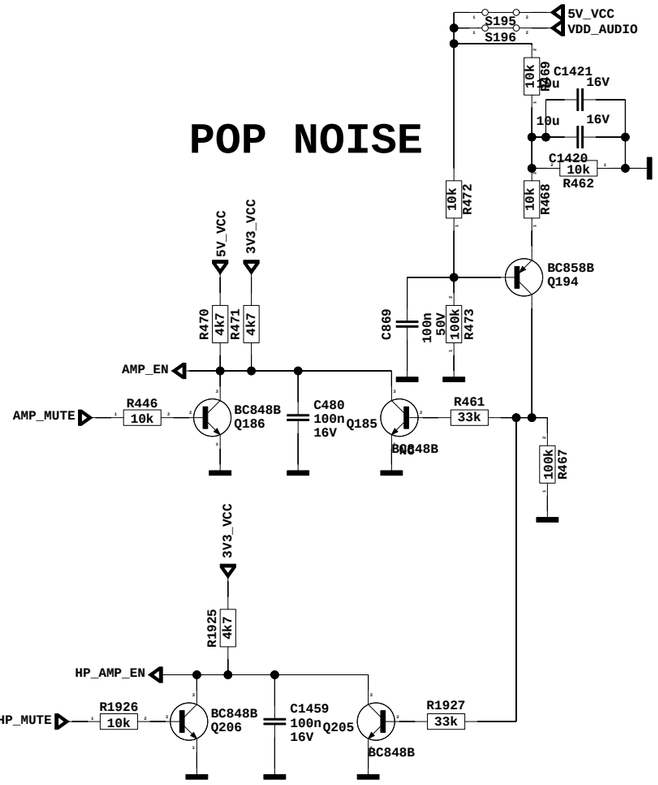




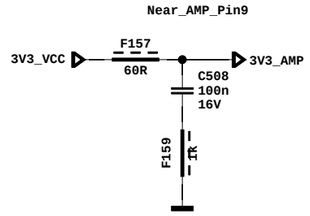


VESTEL	PROJECT NAME : 17mb171-r2a	A3
	SCH NAME :CI_NAND	T. SHT 11
	DRAWN BY :<YOUR NAME HERE>	25/12/2019:13:58

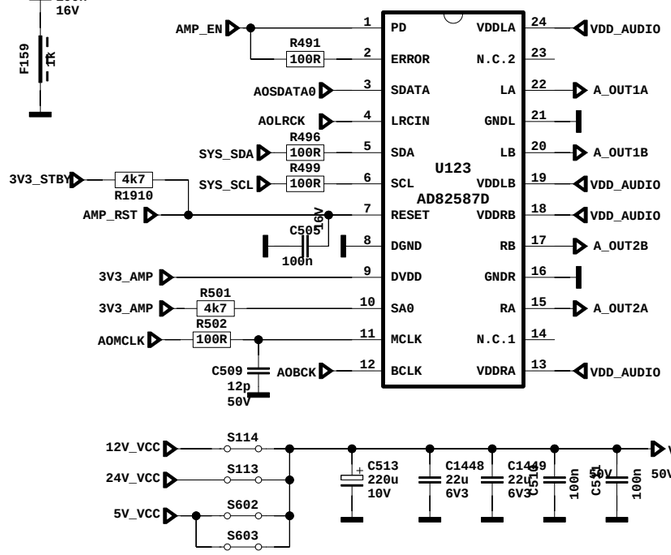
POP NOISE

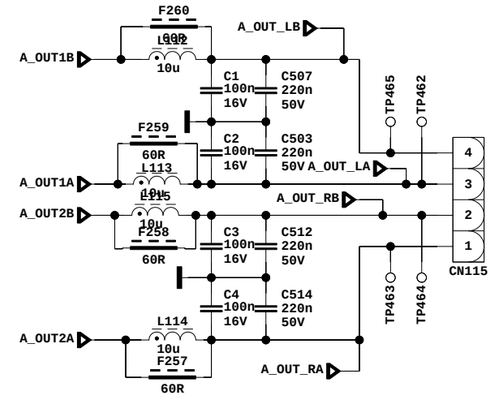


Near_AMP_Pin9

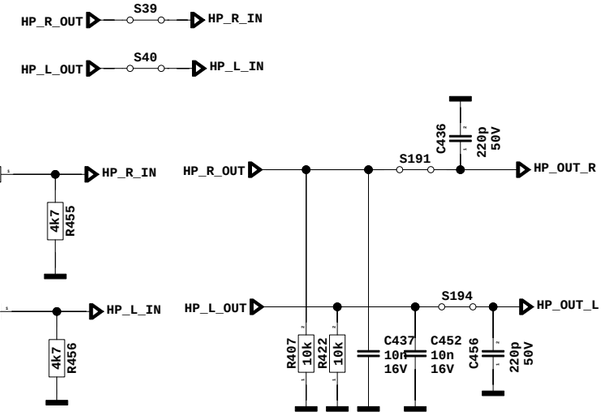


MAIN AMP 6W/8W/10W

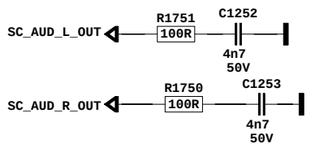




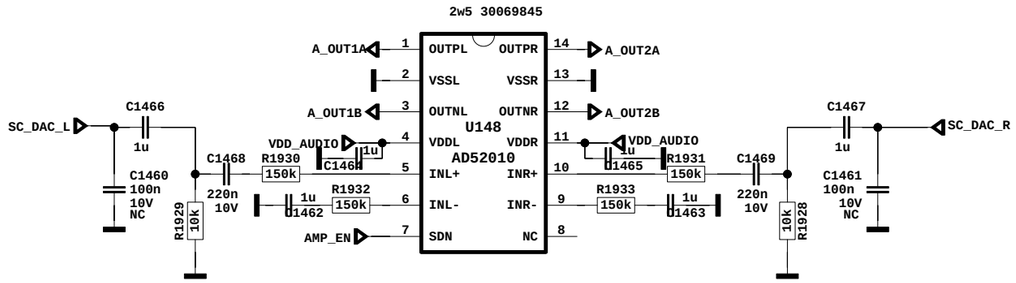
HEADPHONE



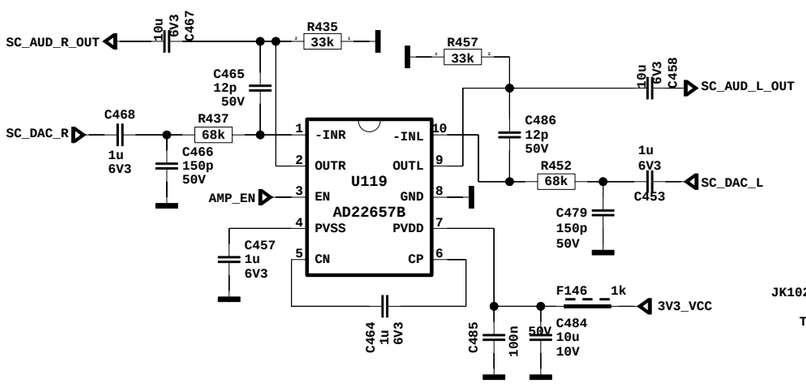
AUDIO AMP for 16" to 24"



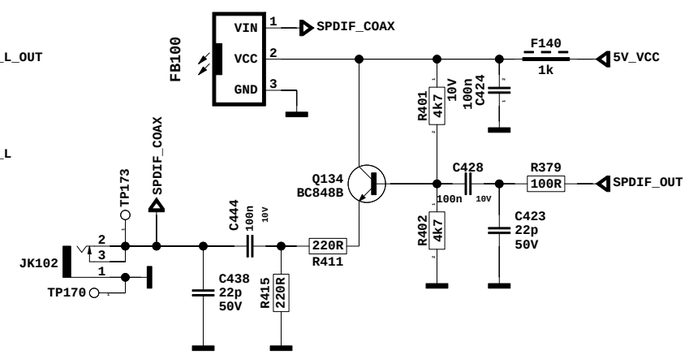
2w5 30069845



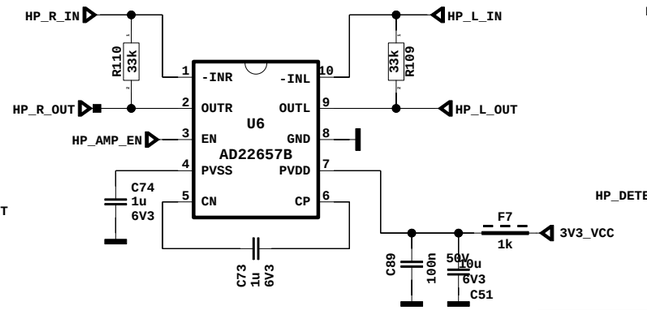
SCART AUDIO AMP



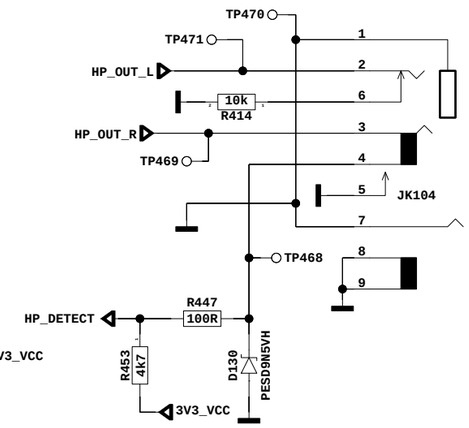
SPDIF OUT



HEADPHONE AMP



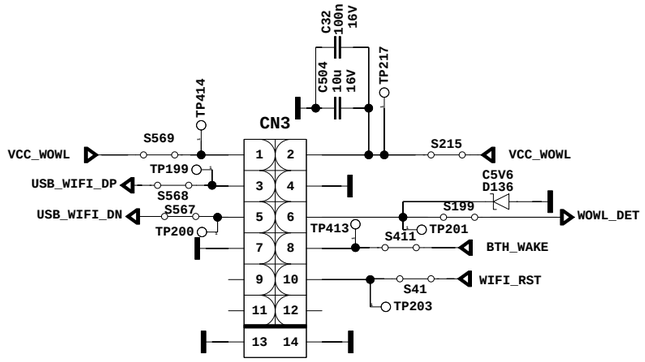
HEADPHONE OUTPUT



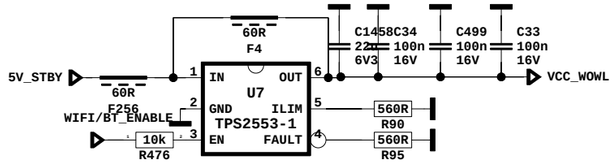
VESTEL	PROJECT NAME : 17mb171-r2a	A3
SCH NAME :AUDIO AMP		T. SHT 11
DRAWN BY :<YOUR NAME HERE>		25/12/2019:13:58

100R

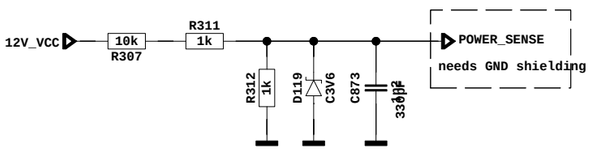
WIFI&BT

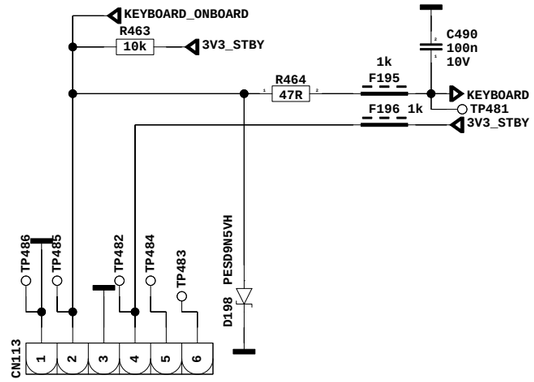


WOWL OPTION

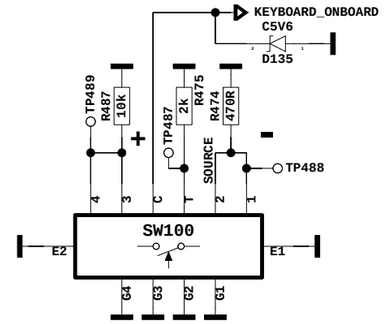


LED





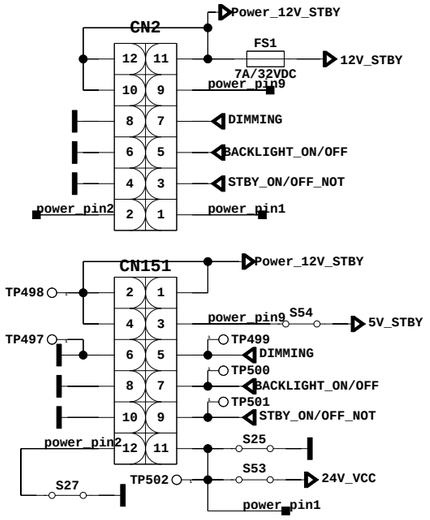
KEYBOARD

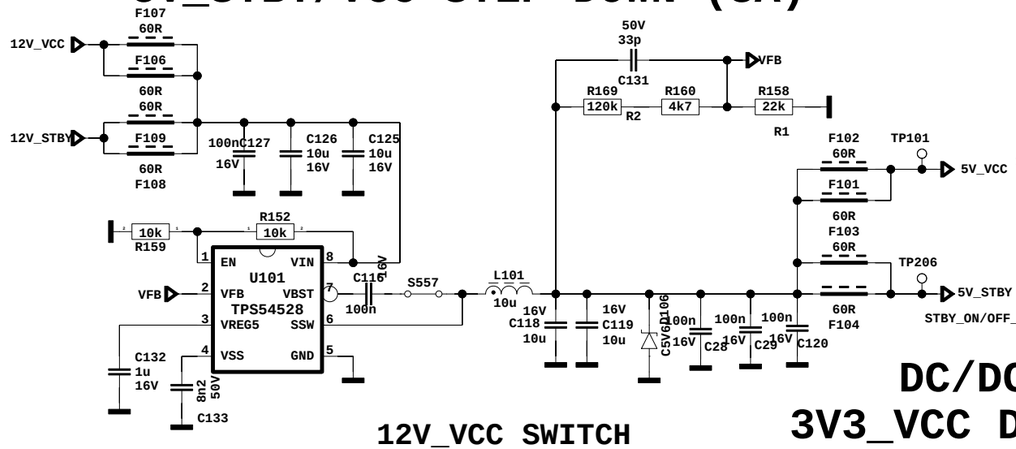


3-WAY

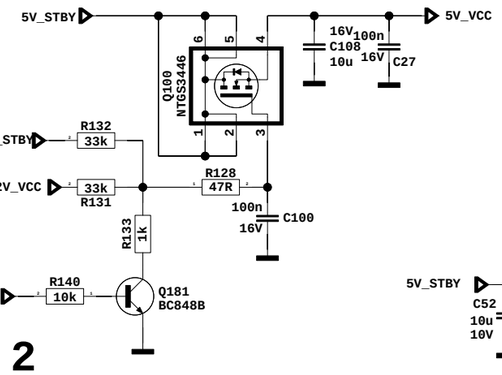
VESTEL	PROJECT NAME : 17mb171-r2a	A3
SCH NAME :CONN_WIFI		T. SHT 11
DRAWN BY :<YOUR NAME HERE>		25/12/2019:13:58

DC/DC 1
5V_STBY/VCC STEP-DOWN (3A)

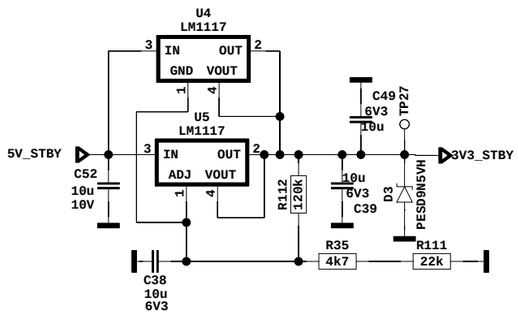




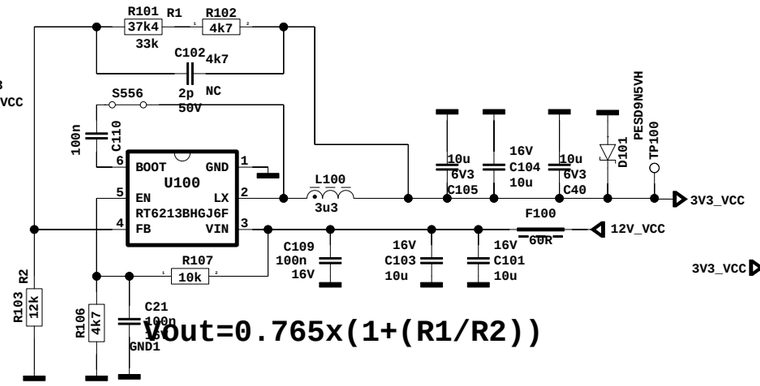
SW2
5V_VCC SWITCH



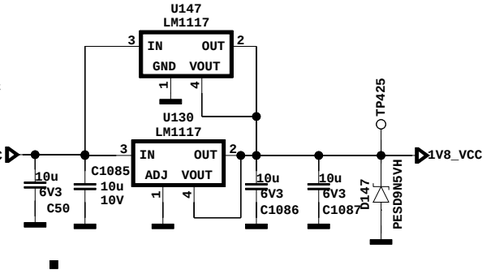
3V3_STBY



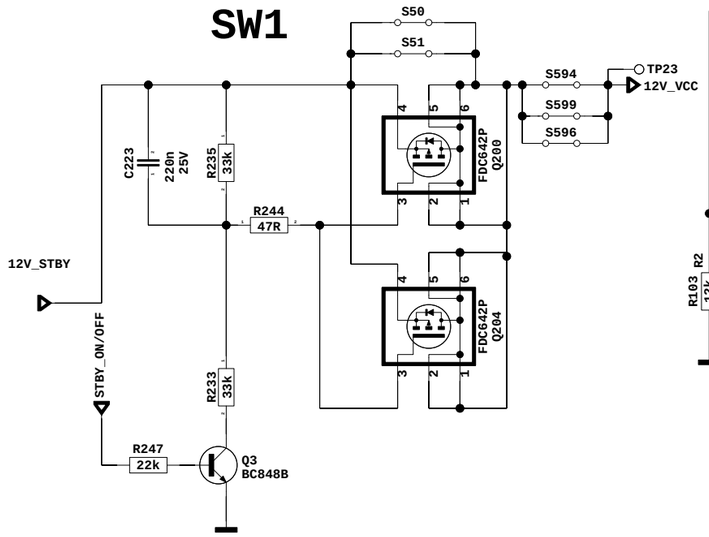
DC/DC 2
3V3_VCC DC/DC (3A)



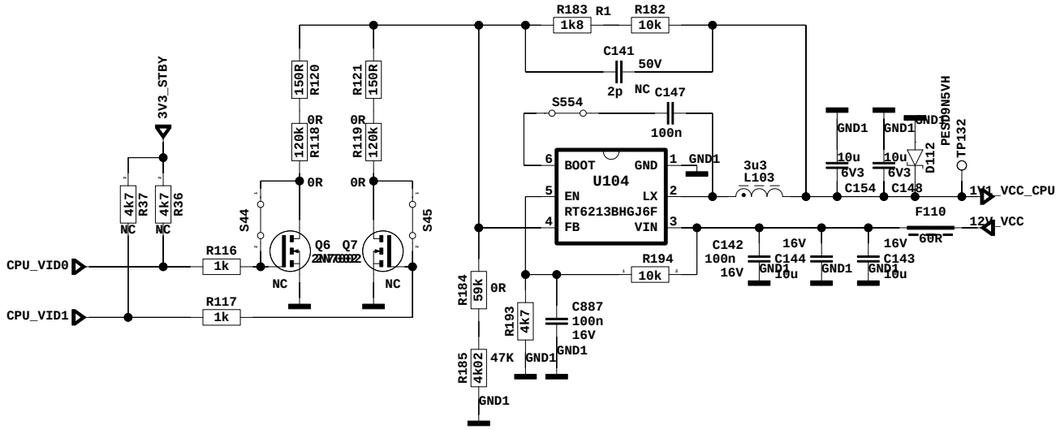
1V8_VCC LDO



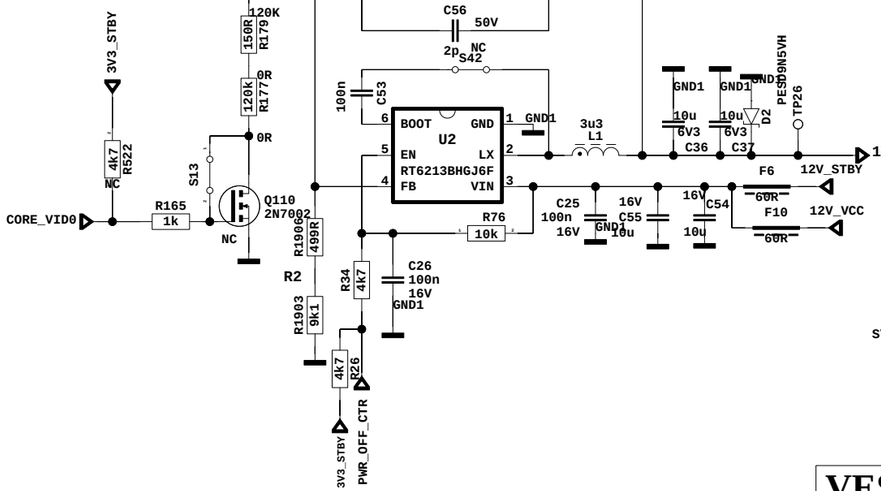
SW1
12V_VCC SWITCH



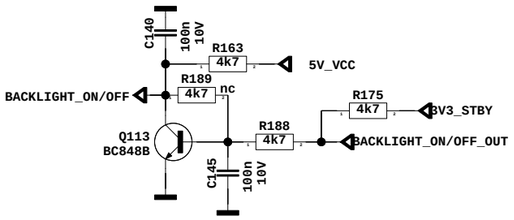
DC/DC 3
1V_VCC_CPU DC/DC (2A)



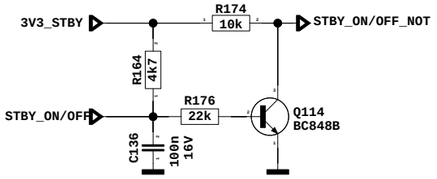
1V_VCC_CORE (3A)



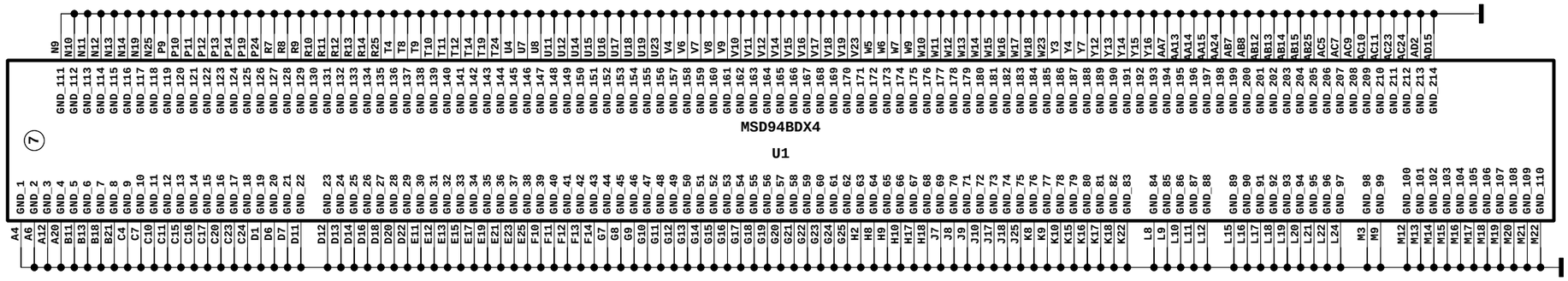
Backlight On/Off Circuit

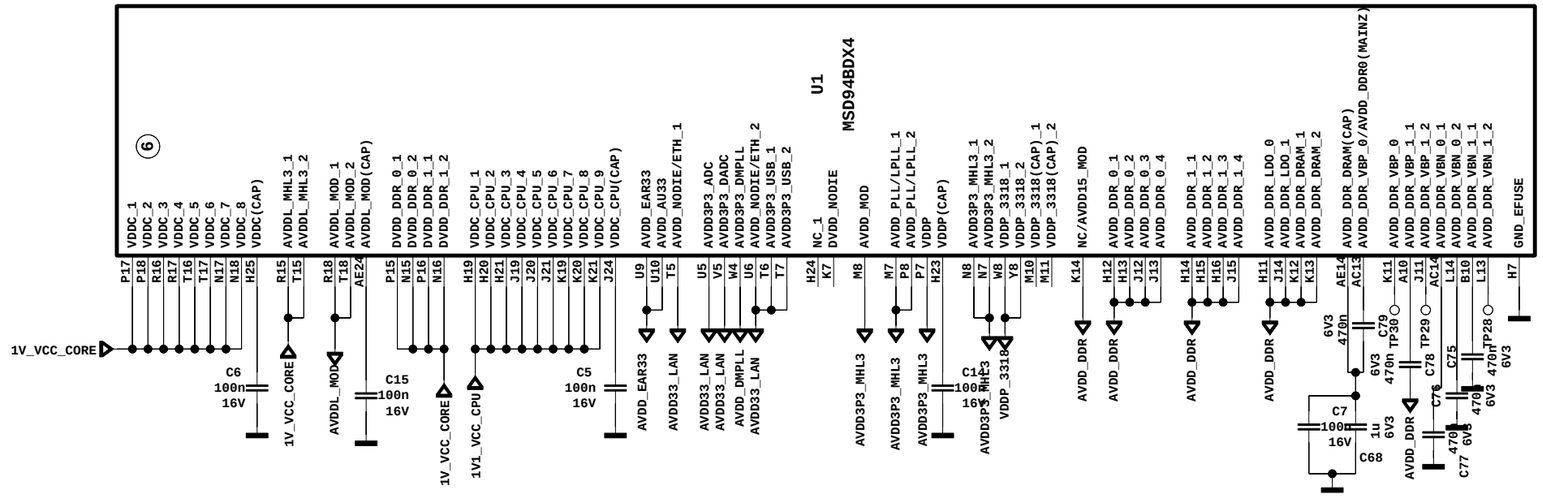


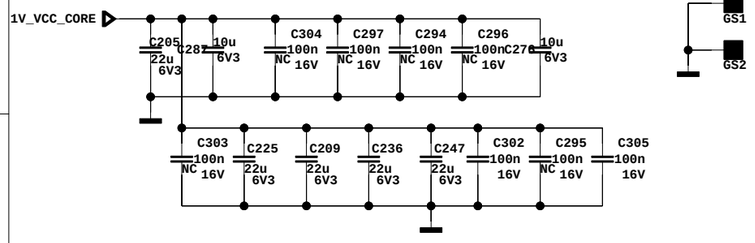
STBY On/Off Circuit

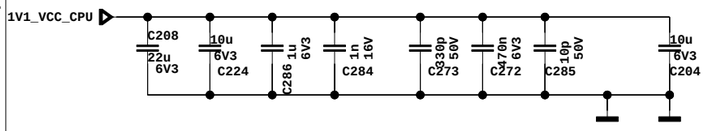


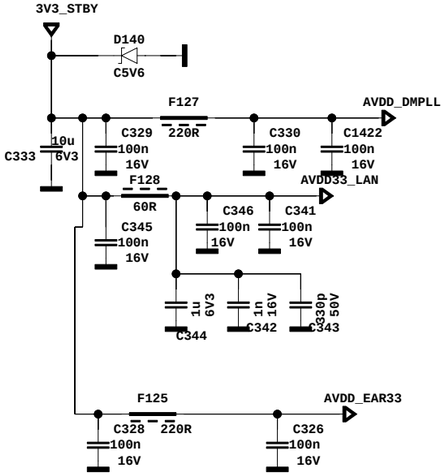
VESTEL	PROJECT NAME : 17mb171-r2a	A3
SCH NAME :POWER		T. SHT 11
DRAWN BY :<YOUR NAME HERE>		25/12/2019:13:58

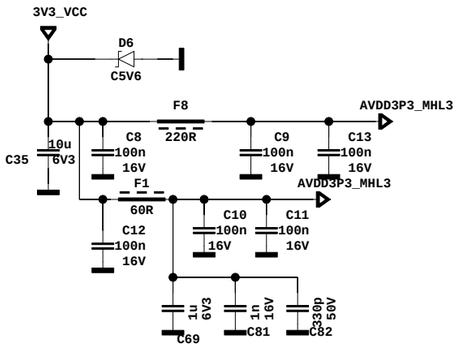


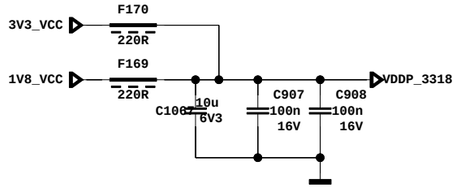


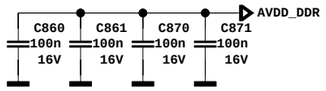


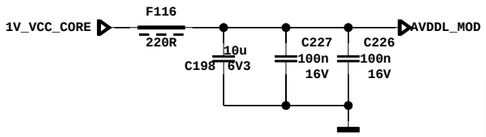












VESTEL	PROJECT NAME : 17mb171-r2a	A3
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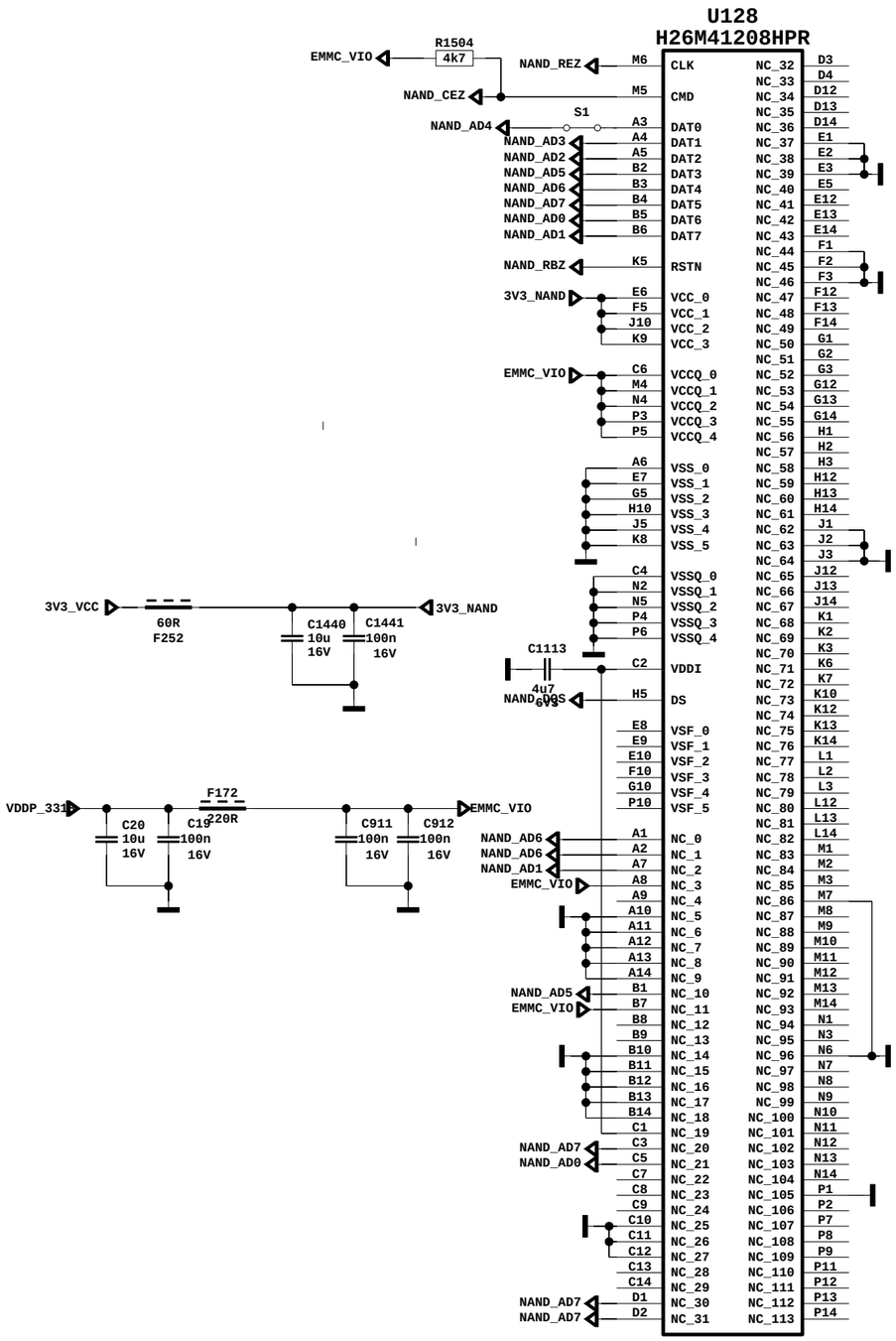
DRAWN BY :<YOUR NAME HERE>		25/12/2019:13:58



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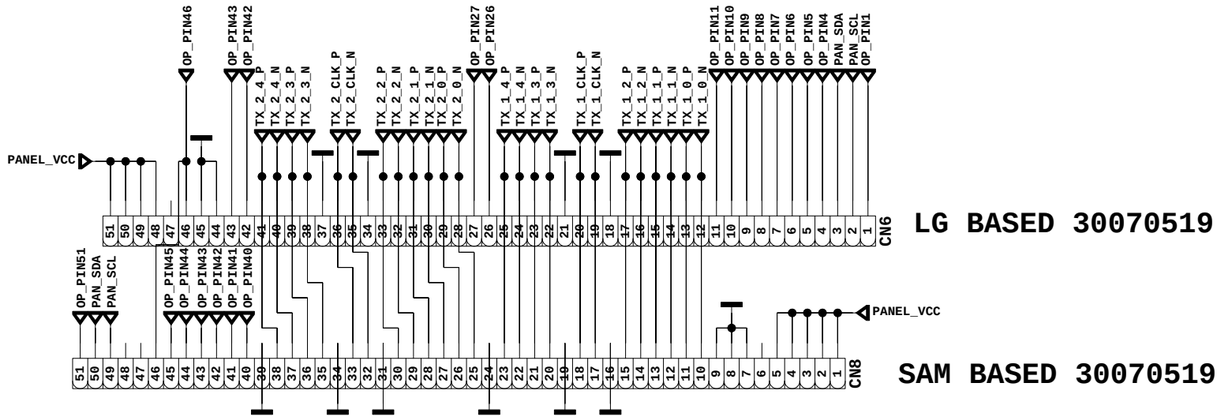
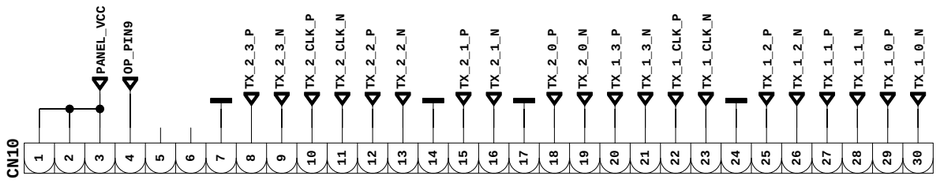
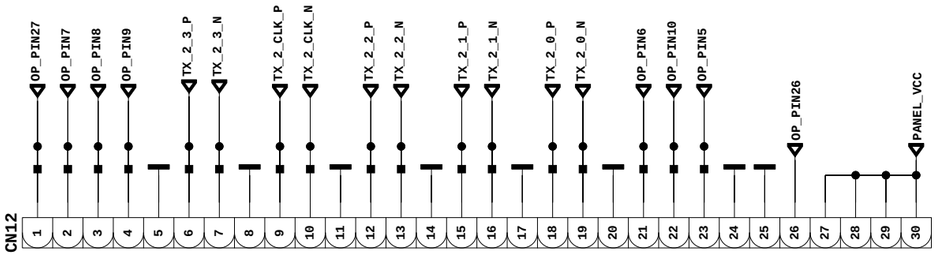
FHD 50Hz 3D FFC



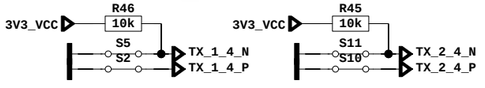
19" TO 22" DOUBLE LVDS FFC OPTIONS



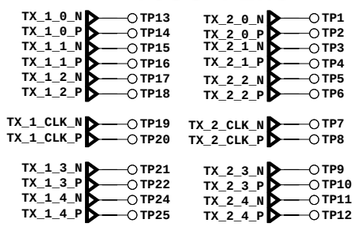
WXGA FFC



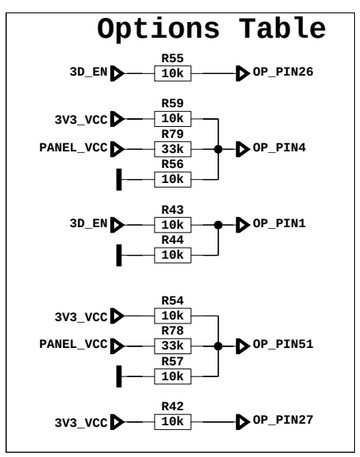
10_BIT PANEL



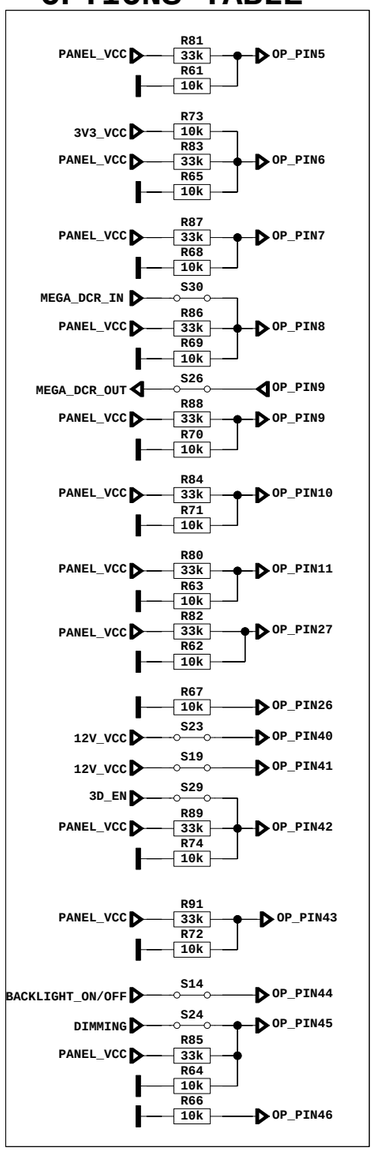
Test Pins



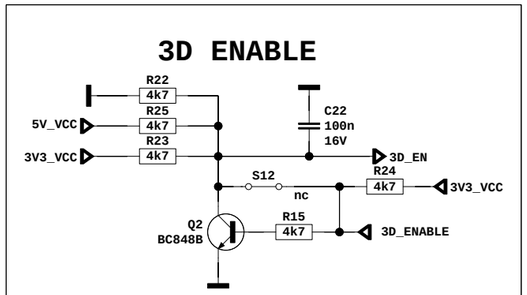
Options Table



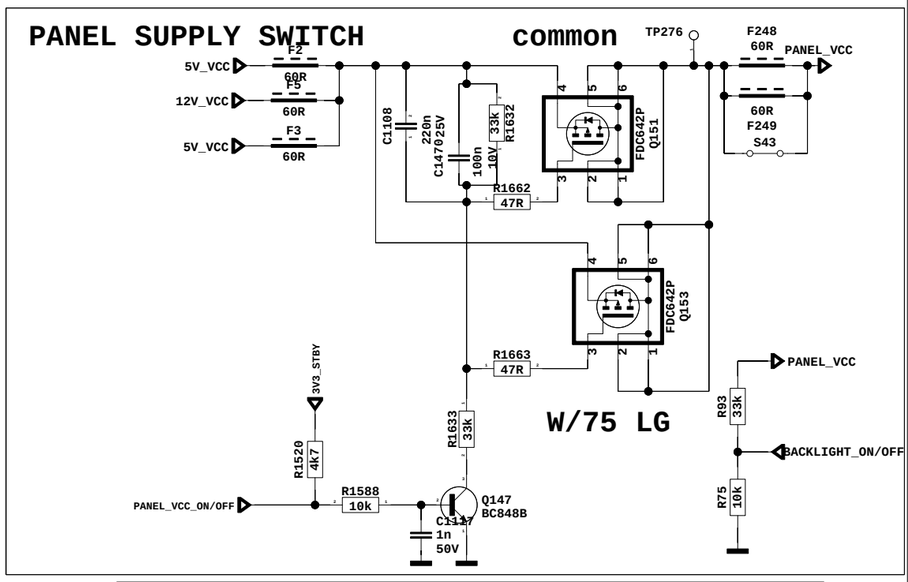
OPTIONS TABLE



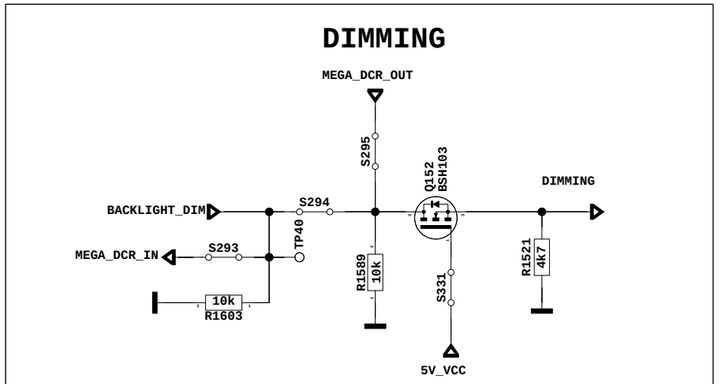
3D ENABLE



PANEL SUPPLY SWITCH



DIMMING



PANEL I2C BUFFER