MB185 IDTV
SERVICE MANUAL

Table of Contents

IMPORTANT

Before removing the rear cover from the TV for servicing, make sure that no cables are fixated to the cover. Release the cables from their clamps and disconnect (if any). Failure to do so may damage the wires and/or other components of the TV.

1. INTRODUCTION

17MB185 main board is driven by MTK SOC. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU.

This board can be driven 50Hz UHD panels.

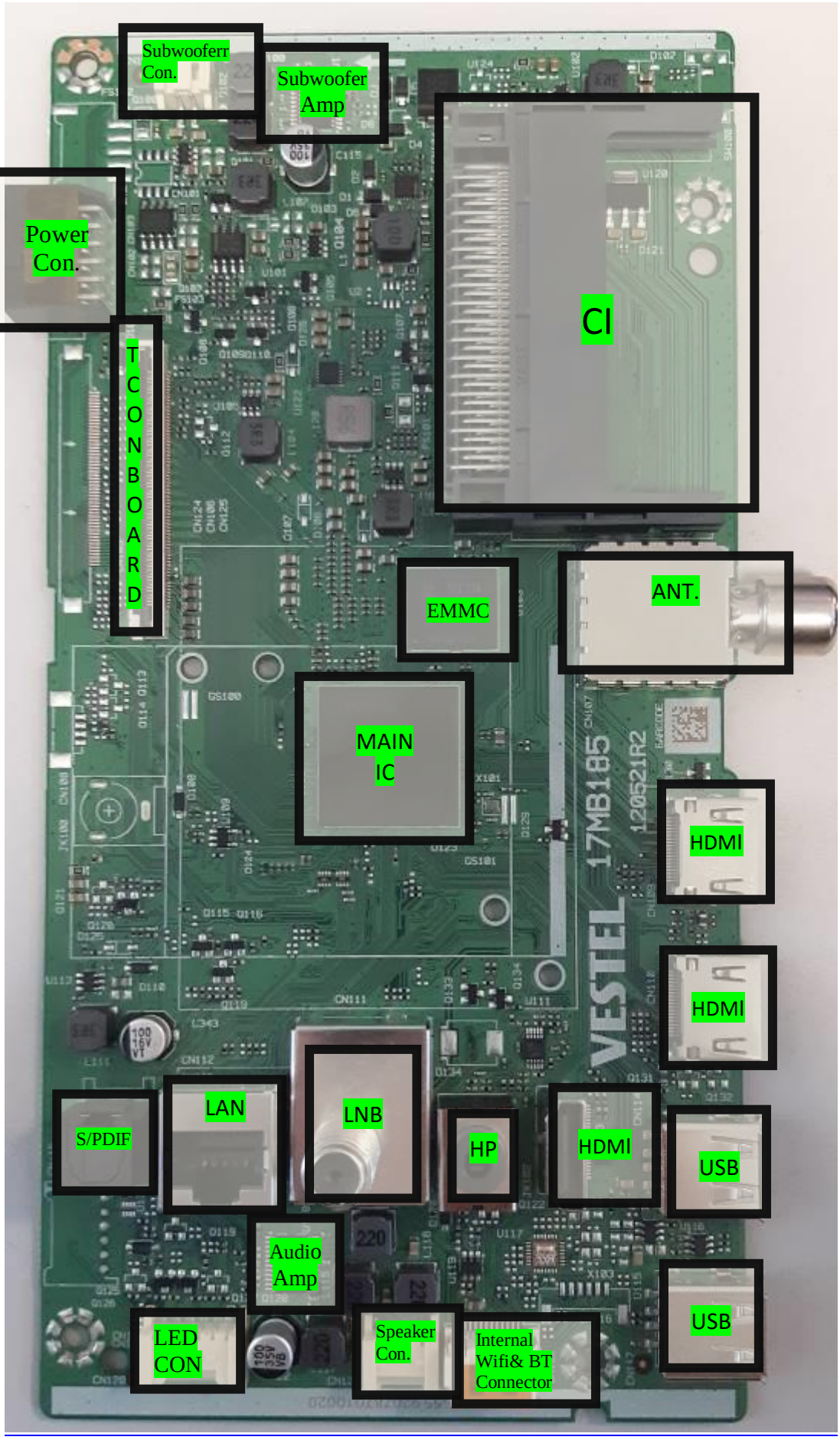
Key features include:

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- The MACEpro video processor
- Home theatre sound processor
- Rich internet connectivity and completed digital home network solution
- Dual-stream decoder for 3D contents
- Multi-purpose CPU for OS and multimedia
- Peripheral and power management
- Embedded DRAM (for connected option)

Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Sub-woofer sound socket
- 3x HDMI inputs (2x side , 1x back side)(with ARC option from 2nd or 3rd input)
- 1 Common interface(Common)
- 1 Optic/ Quax S/PDIF output
- 1 Headphone(Common)
- 2x USB(2X Side) and 1x internal USB for Wifi/Bluetooth
- 1 Ethernet-RJ45
- 1 External Keypad/Tact Switch

SSB LAYOUT


Subwooferr Con.
Subwoofer Amp
Power Con.
CI
TCONBOARD
EMMC
ANT.
MAIN IC
HDMI
HDMI
S/PDIF
LAN
LNB
HP
HDMI
USB
Audio Amp
USB
LED CON
Speaker Con.
Internal Wifi& BT Connector

2. T/T2/C/A TUNER (U107)

Description:

The Si2151 is Silicon Labs' sixth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wirewound inductors or LNAs, the Si2151 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2151 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners. The Si2151 offers increased immunity to WiFi and LTE interference, eliminating the need for external filtering. For the best performance with next-generation digital TV standards, such as DVB-T2/C2, the Si2151 delivers industry-leading phase noise performance.

Features:

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVBT2/T/C2/C, ISDB-T/C, DTMB
- 1.7 MHz, 6 MHz, 7 MHz, 8 MHz, and 10 MHz channel bandwidths
- 42-1002 MHz frequency range
- Industry-leading margin to A/74, NorDig, DTG, ARIB, EN55020, OpenCable™,DTMB
- Lowest BOM for a hybrid TV tuner
  - No balun, SAW filters, or external inductors required
  - Increased ESD protection on 4pins
- Best-in-class real-world reception
  - Lowest phase noise
  - High Wi-Fi and LTE immunity
- Low power consumption
  - 3.3 V and 1.8 V power supplies
  - Integrated 1.8 V LDO for 3.3 V singlesupply operation
- Integrated power-on reset circuit
- Standard CMOS process
- 3x3 mm, 24-pin QFN package
- RoHS compliant

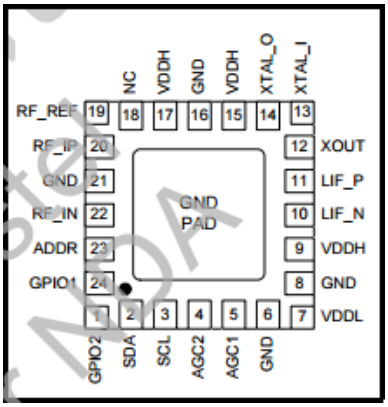


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Figure 1: Si2151 Pin description

Pin Number(s)	Name	I/O	Description
1*	GPIO2	I/O	General purpose input/output #1
2	SDA	I/O	I^2C data input/output
3	SCL	I	I^2C clock input
4*	AGC2	I	LIF output amplitude control input #2
5*	AGC1	I	LIF output amplitude control input #1
6	GND	S	Ground
7	VDDL	S	Low supply voltage, 1.8 V (leave caps connected for single supply case)
8	GND	S	Ground
9	VDDH	S	High supply voltage, 3.3 V
10	LIF_N	O	Negative LIF differential output to SoC or DTV/ATV demodulator
11*	LIF_P	O	Positive LIF differential output to SoC or DTV/ATV demodulator
12	XOUT	O	Output reference clock to secondary tuner or receiver
13	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)
14	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)
15	VDDH	S	High supply voltage, 3.3 V
16	GND	S	Ground
17	VDDH	S	High supply voltage, 3.3 V
18*	NC	NC	No connect
19	RF_REF	O	RF reference voltage output
20	RF_IP	I	RF input (positive)
21	GND	S	Ground
22	RF_IN	I	RF input (negative)
23	ADDR	I	I^2C address select
24*	GPIO1	I/O	General purpose input/output #1
***Note:** Pin should be left floating if unused.			

3. S/S2 TUNER (U3) OPTIONAL

Description

M88TS6011 is a single-chip, direct-conversion tuner for digital satellite receiver applications. It offers the industry's most integrated solution to a satellite tuner function, simplifying the front-end designs.

This device incorporates the following functional blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with an integrated auxiliary clock output.

As a result of integrating all these blocks, the M88TS6011 has the least number of pins compared with other conventional solutions, and requires the least external components. In typical applications, the M88TS6011 requires only one crystal, one matching network, and a few external capacitors. The device also has the industry's smallest latency, as it uses a fast locking PLL and a fast settling DC offset cancellation architecture.

The M88TS6011 can be configured via a 2-wire serial bus. The chip is available in a 16-pin QFN package.

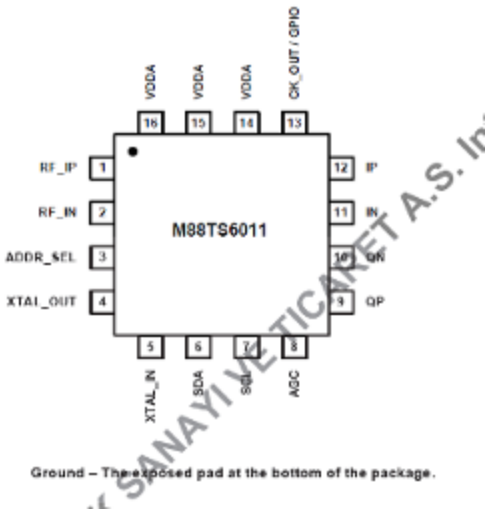
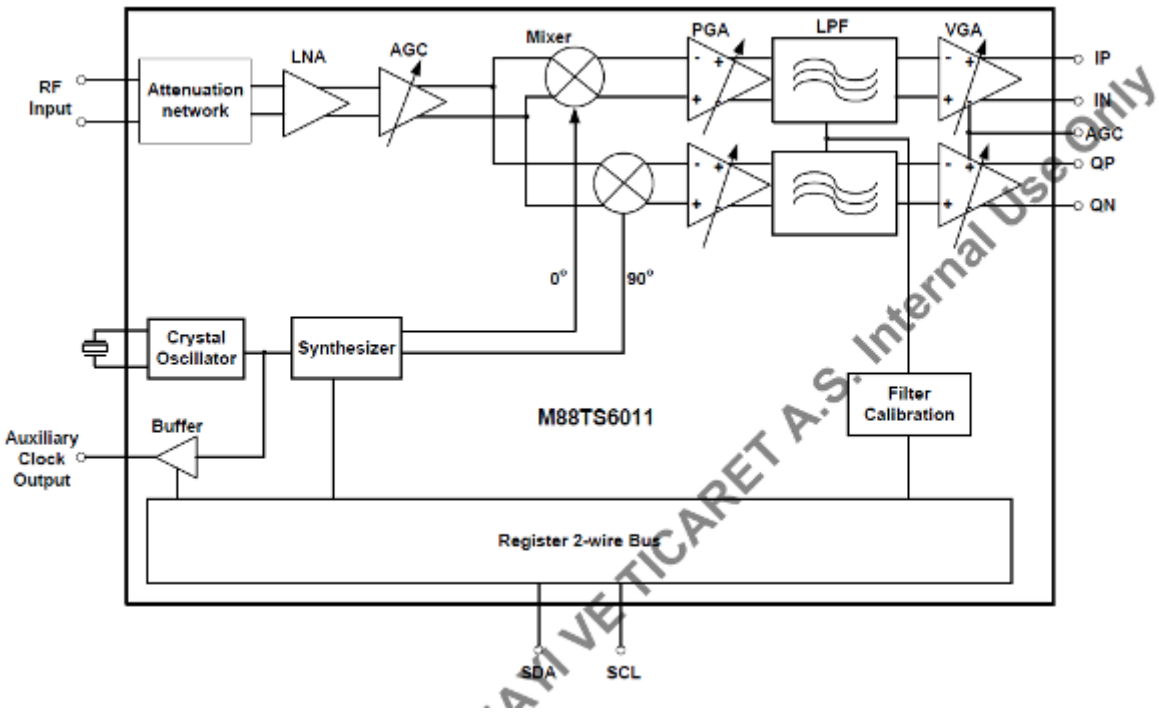


Figure 2: Pin description

Features

- Single-chip tuner
- Compliant with DVB-S/S2 and ABS-S standards
- Support QPSK, 8PSK, 16APSK and 32APSK
- Direct-conversion from L-band to baseband
- Symbol rate: 1 to 45 Msymbol/s
- Integrated VCOs and PLL, with on-chip inductors, varactors and loop filter
- Integrated baseband filters: 6 MHz to 40 MHz bandwidth
- Integrated RF AGC for optimal performance
- Integrated baseband DC offset cancellation removes external loop filters
- Excellent immunity to strong adjacent undesired channels
- Integrated clock driver provides auxiliary clock output for other devices
- Support sleep mode
- 2-wire serial bus with 3.3 V compatible logic levels
- Power supply: +3.3 V
- Package:16-pin E-PAD QFN
- RoHS compliant

Block Diagram



4. AUDIO AMPLIFIER STAGES

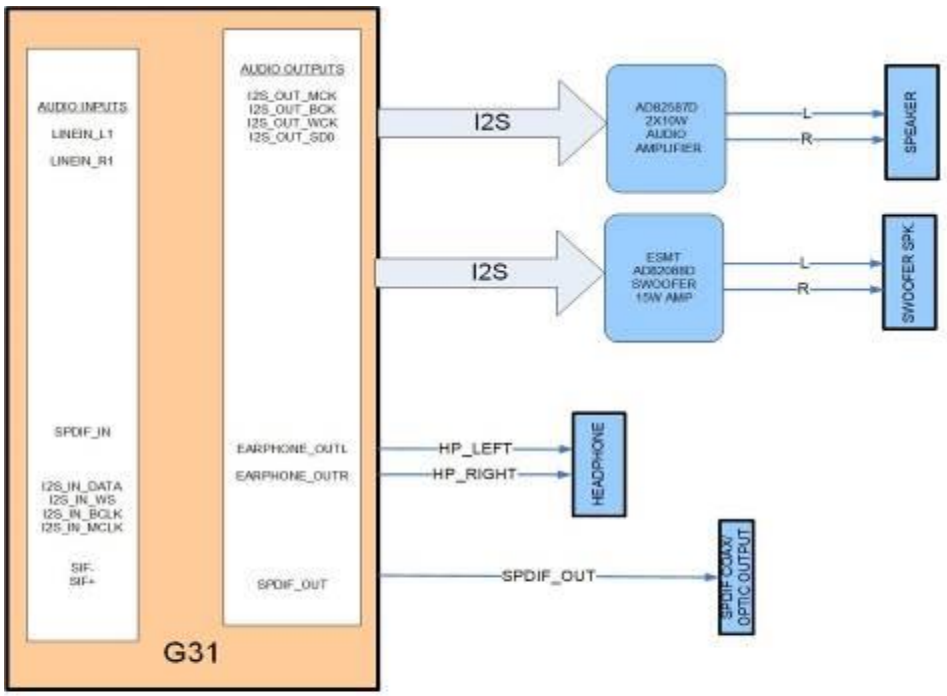


Figure: The block diagram of the audio part

A. *MAIN AMPLIFIER (U118) (8W/10W/12W OPTİONS)*

Description

AD82587D is a digital audio amplifier capable of driving a pair of 8 ohm, 20W or a single 4 ohm, 40W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I^2C digital control interface, the user can control AD82587D's input format selection, DRC (dynamic range control), mute and volume control functions. AD82587D has many built-in protection circuits to safeguard AD82587D from connection errors.

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting) Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  - 32kHz / 44.1kHz / 48kHz and
  - 64kHz / 88.2kHz / 96kHz and
  - 128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x,1024x Fs
  - 256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  - 128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  - 64x~256x Fs for 128kHz /176.4kHz/192kHz
- Supply voltage
  - 3.3V for digital circuit

  - 10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
  - 10W x 2ch into 8_ @ 0.16% THD+N
  - 15W x 2ch into 8_ @ 0.18% THD+N
  - 20W x 2ch into 8_ @ 0.24% THD+N
- Loudspeaker output power for Mono@ 24V
  - 20W x 1ch into 4_ @ 0.17% THD+N
  - 30W x 1ch into 4_ @ 0.2% THD+N
  - 40W x 1ch into 4_ @ 0.24% THD+N
- Sounds processing including:
  - Volume control (+24dB~-103dB, 0.125dB/step)
  - Dynamic range control
  - Power clipping
  - Channel mixing
  - User programmed noise gate with hysteresis window
  - DC-blocking high-pass filter

- Anti-pop design
- Short circuit and over-temperature protection
- I2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage
- detection
- Power saving mode
- Dynamic temperature control

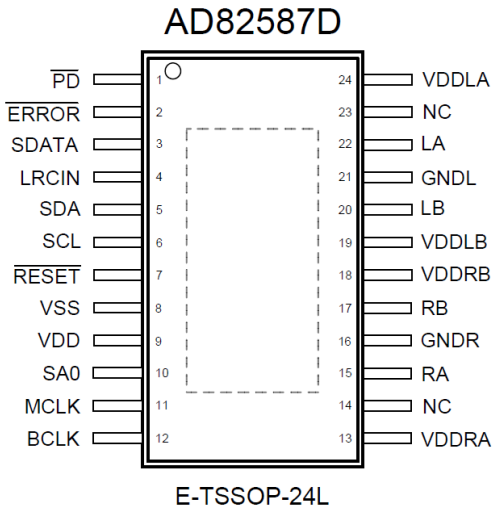


Figure 3: Pin description

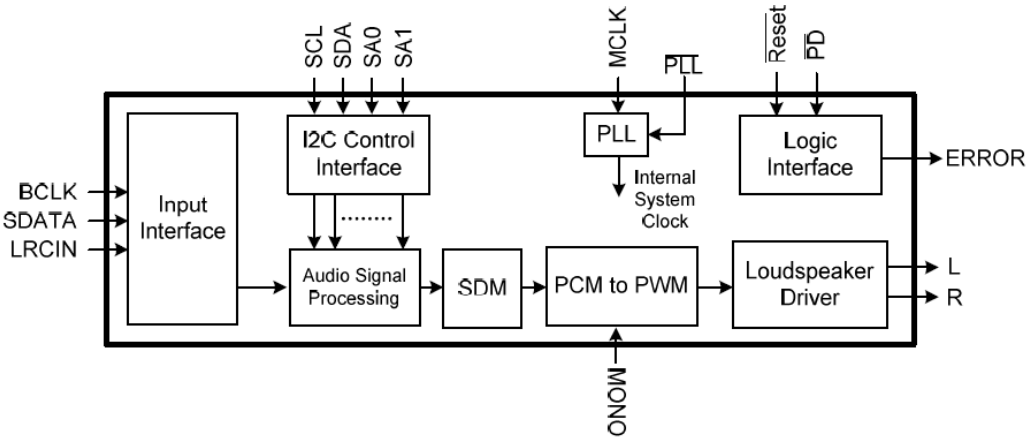


Figure 4: Functional Block Diagram

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_J	Junction Operating Temperature	0~125	°C
T_A	Ambient Operating Temperature	0~70	°C

Table 2: Recommended Operating Conditions

B. SUB-WOOFER AMPLIFIER (U1)

ESMT *AD82088*

2x20W Stereo / 1x40W Mono Digital Audio Amplifier With 30 bands EQ and DRC Functions

Features

- Supply voltage
  3.3V for digital circuit
  8V~26V for loudspeaker driver
- Supports 2.0CH/Mono configuration
- Loudspeaker output power@12V for stereo
  7W x 2CH into 8Ω <1% THD+N
  10W x 2CH into 4Ω <1% THD+N
- Loudspeaker output power@18V for stereo
  15W x 2CH into 8Ω <1% THD+N
- Loudspeaker output power@24V for stereo
  20W x 2CH into 8Ω <1% THD+N
- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  MCLK system:
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz / 176.4kHz / 192kHz
  BCLK system:
  64xFs for 32kHz / 44.1kHz / 48kHz
  64xFs for 64kHz / 88.2kHz / 96kHz
  64xFs for 128kHz / 176.4kHz / 192kHz
- Sound processing including :
  30 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Three Band plus post Dynamic range control
  Power Clipping
  Programmed 3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  Bass/Treble tone control
  DC-blocking high-pass filter
  Pre-scale/post-scale
- Supports I^2C control without clock
- I^2C control interface with selectable device address
- I^2S output with selectable Audio DSP point
- Support hardware and software reset
- Internal PLL
- Anti-pop design
- Level meter and power meter
- LV Under-voltage shutdown and HV Under-voltage detection
- Over voltage protection
- Short circuit and over-temperature protection

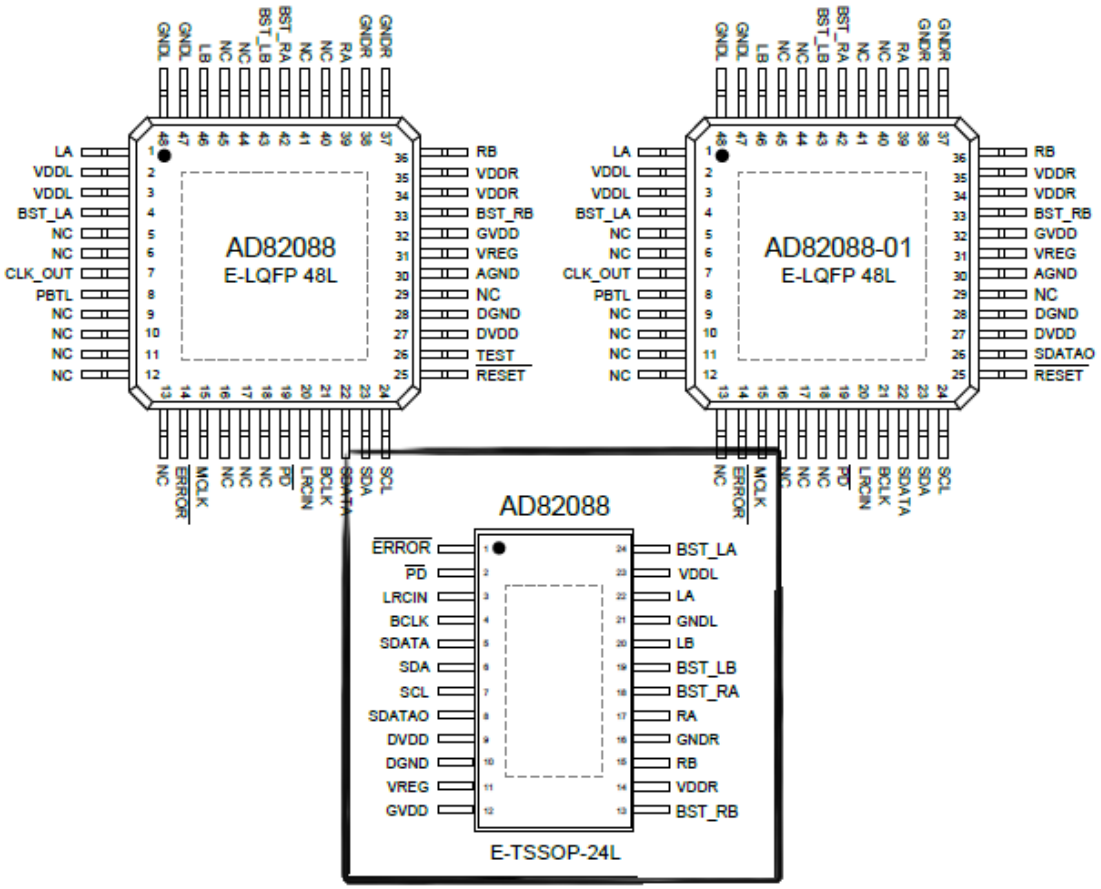
Applications

- TV audio

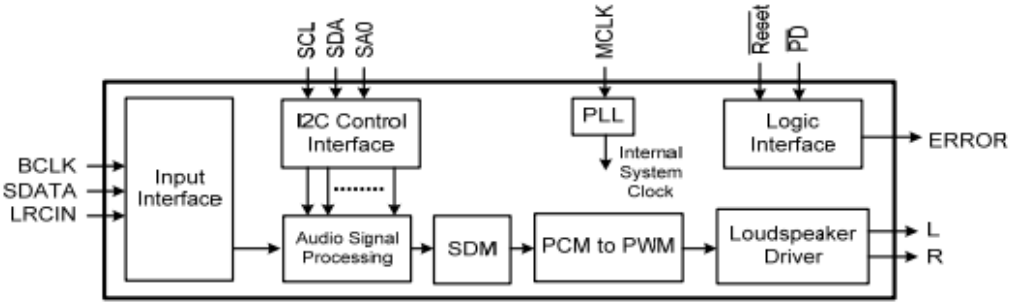
Description

AD82088 is a digital audio amplifier capable of driving 20W (BTL) each to a pair of 8Ω load speaker and 40W (PBTL) to a 4Ω load speaker operating at 24V supply without external heat-sink or fan requirement with play music. AD82088 provides advanced audio processing functions, such as volume control, 30 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC). These are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD82088 from damage due to accidental erroneous operating condition. The full digital circuit design of AD82088 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog class-AB or class-D audio amplifier counterpart implemented by analog circuit design. AD82088 is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment



Functional Block Diagram



Pin Description (E-TSSOP 24L)

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	$\overline{\text{ERROR}}$	I/O	$\overline{\text{ERROR}}$ pin is a dual function pin. One is I^2C address setting during power up. The other one is error status report (low active), It sets by register of A_SEL_FAULT at address 0x1C B[6] to enable it.	This pin is monitored on the rising edge of reset. A value of Low (15-kΩ pull down) sets the I^2C device address to 0x30 and a value of High (15-kΩ pull up) sets it to 0x31.
2	$\overline{\text{PD}}$	I	Power down, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
3	LRCIN	I	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
4	BCLK	I	Bit clock input (64Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
5	SDATA	I	Serial audio data input.	Schmitt trigger TTL input buffer
6	SDA	I/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
7	SCL	I	I^2C serial clock input.	Schmitt trigger TTL input buffer
8	SDATAO	O	Serial audio data output.	Schmitt trigger TTL input buffer
9	DVDD	P	Digital Power.	
10	DGND	P	Digital Ground.	
11	VREG	O	1.8V Regulator voltage output.	
12	GVDD	O	5V Regulator voltage output. This pin must not be used to drive external devices.	
13	BST_RB	P	Bootstrap supply for right channel output B.	
14	VDDR	P	Right channel supply.	
15	RB	O	Right channel output B.	
16	GNDR	P	Right channel ground.	
17	RA	O	Right channel output A.	
18	BST_RA	P	Bootstrap supply for right channel output A.	
19	BST_LB	P	Bootstrap supply for left channel output B.	
20	LB	O	Left channel output B.	
21	GNDL	P	Left channel ground.	
22	LA	O	Left channel output A.	
23	VDDL	P	Left channel supply.	
24	BST_LA	P	Bootstrap supply for left channel output A.	

5. POWER STAGE

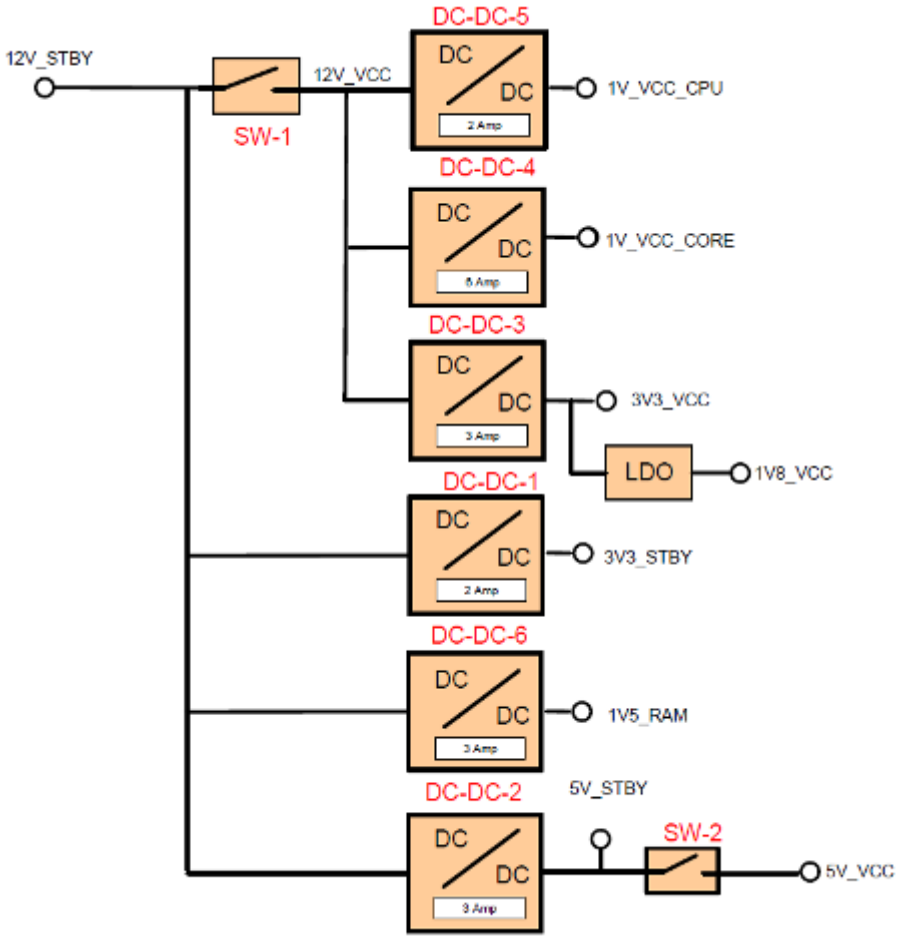


Figure: Power Block Diagram

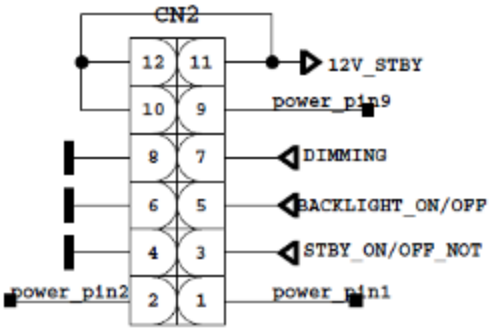


Figure: Power Socket and Power Options

Power socket is used for taking 12V_STBY voltage which is produced in power card. Also socket is used for giving dimming, backlight and standby signals with power card. Power socket pinning is shown in above figure.

12V_STBY is converted several different voltages on the mainboard which are shown in below figure.

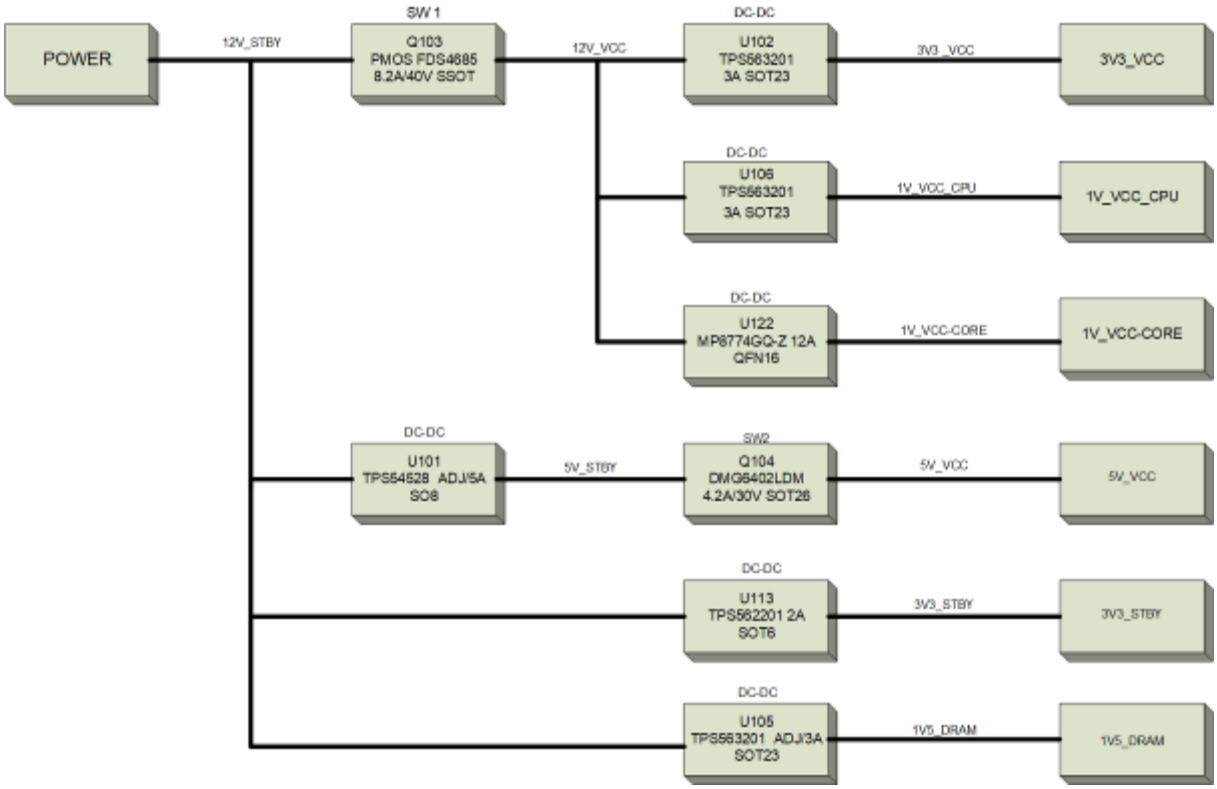


Figure: Power Block Diagram

List of the components:

- SW-1(Q103) → FDS4685 8.2A/40V
- SW-2(Q104) → DMG8402LDM 4.2A/30V
- DC-DC-1(U101) → TPS54528 ADJ/5A
- DC-DC-2(U102) → TPS563201 ADJ/3A
- DC-DC-3(U105) → TPS563201 ADJ/3A
- DC-DC-4(U106) → TPS563201 ADJ/3A
- DC-DC-5(U113) → TPS562201 ADJ/2A
- DC-DC-6(U122) → MP8774GQ-Z 12A

A. *FDS4685 8.2A/40V (Q103)*

FAIRCHILD
SEMICONDUCTOR®

FDS4685
40V P-Channel PowerTrench® MOSFET

Features

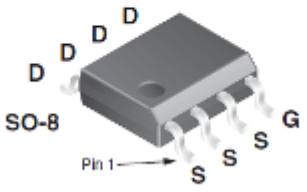
- –8.2 A, –40 V $R_{DS(ON)}$ = 0.027 Ω @ V_{GS} = –10 V
  $R_{DS(ON)}$ = 0.035 Ω @ V_{GS} = –4.5 V
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

Applications

- Power management
- Load switch
- Battery protection

General Description

This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V – 20V).



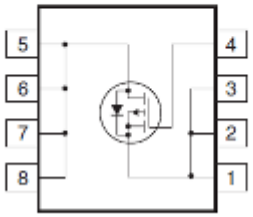


Figure: Pin description

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA	–40			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		–32		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –32 V, V_{GS} = 0 V			–1	µA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–1	–1.6	–3	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		4.7		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –10 V, I_D = –8.2 A V_{GS} = –4.5 V, I_D = –7 A V_{GS} = –10 V, I_D = –8.2 A, T_J = 125°C		22 29 31	27 35 42	mΩ
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –8.2 A		22		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –20 V, V_{GS} = 0 V, f = 1.0 MHz		1872		pF
C_{oss}	Output Capacitance			256		pF
C_{rss}	Reverse Transfer Capacitance			134		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1MHz		4		Ω

Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –20 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω		14	25	ns
t_r	Turn–On Rise Time			11	20	ns
$t_{d(off)}$	Turn–Off Delay Time			50	80	ns
t_f	Turn–Off Fall Time			18	32	ns
Q_g	Total Gate Charge	V_{DS} = –20 V, I_D = –8.2 A, V_{GS} = –5 V		19	27	nC
Q_{gs}	Gate–Source Charge			5.6		nC
Q_{gd}	Gate–Drain Charge			6.1		nC
Drain–Source Diode Characteristics						
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –2.1 A (Note 2)		–0.7	–1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = –8.2 A, d_{IF}/d_t = 100 A/μs		26		nS
Q_{rr}	Diode Reverse Recovery Charge			15		nC

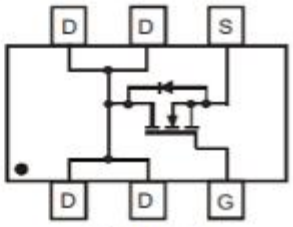
B. DMG8402LDM (Q104)

Features

- Low RDS(ON)
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Lead Free By Design/RoHS Compliant (Note 1)
- Qualified to AEC-Q101 Standards for High Reliability

SOT-26

TOP VIEW



TOP VIEW
Internal Schematic

Pin description

Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 5)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current T_J = 25°C	I_{DSS}	-	-	1.0	μA	V_{DS} = 30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.5	2.0	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	-	22 32	27 40	mΩ	V_{GS} = 10V, I_D = 7A V_{GS} = 4.5V, I_D = 5.6A
Forward Transfer Admittance	$\|Y_{fs}\|$	-	10	-	S	V_{DS} = 5V, I_D = 7A
Diode Forward Voltage	V_{SD}	-	0.75	1.0	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 6)						
Input Capacitance	C_{iss}	-	404	-	pF	V_{DS} =15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	52	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	45	-	pF	
Gate Resistance	R_g	-	1.51	-	Ω	V_{DS} =0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	-	9.2	-	nC	V_{GS} =10V, V_{DS} = 15V, ID =5.8A
Gate-Source Charge	Q_{gs}	-	1.2	-	nC	
Gate-Drain Charge	Q_{gd}	-	1.8	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	3.41	-	ns	V_{DD} = 15V, V_{GS} = 10V, R_L = 2.6Ω, R_G = 3Ω
Turn-On Rise Time	t_r	-	6.18	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	13.92	-	ns	
Turn-Off Fall Time	t_f	-	2.84	-	ns	

Notes: 5. Short duration pulse test used to minimize self-heating effect.
6. Guaranteed by design. Not subject to production testing.

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 3)	P_D	1.12	W
Thermal Resistance, Junction to Ambient T_A = 25°C (Note 3)	$R_{\theta JA}$	111	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Notes: 1. No purposefully added lead.
2. Diodes Inc's "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.
3. Device mounted on FR-4 PCB, with minimum recommended pad layout.
4. Repetitive Rating, pulse width limited by junction temperature.

Electrical Characteristics & Maximum ratings

C. TPS54528 (U101)

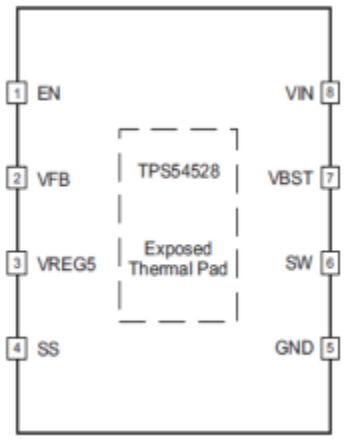
General Description

The TPS54528 is an adaptive on-time D-CAP2™mode synchronous buck converter. The TPS54528 enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54528 uses the D-CAP2™ mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode™ operation at light loads. Eco-mode™ allows the TPS54528 to maintain high efficiency during lighter load conditions. The TPS54528 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 6.0 V. The device also features an adjustable soft start time. The TPS54528 is available in the 8-pin DDA package, and designed to operate from –40°C to 85°C.

Features

- D-CAP2™ Mode Enables Fast Transient Response
- Low Output Ripple and Allows Ceramic Output Capacitor
- Wide VIN Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.76 V to 6.0 V

- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications – 65 mΩ (High Side) and 36 mΩ (Low Side)
- High Efficiency, less than 10 μA at shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 650-kHz Switching Frequency (f_{sw})
- Cycle By Cycle Over Current Limit
- Auto-Skip Eco-mode™ for High Efficiency at Light Load



Pin Assignment

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable Control Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA.
2	FB	Feedback Voltage Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider. The feedback threshold voltage is 0.765V typically.
3	PVCC	Regulator Output for Internal Circuit. Connect a 1μF capacitor to GND to stabilize output voltage.
4	SS	Soft-Start Time Setting. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 3.9nF capacitor sets the soft-start period of V_{OUT} to 2.6ms.
5, 9 (Exposed Pad)	GND	Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.
6	SW	Switch Node. Connect this pin to an external L-C filter.
7	BOOT	Bootstrap Supply for High Side Gate Driver. Connect a 0.1μF or greater ceramic capacitor from BOOT to SW pins.
8	VIN	Power Input. The input voltage range is from 4.5V to 18V. Must bypass with a suitably large (≥10μF x 2) ceramic capacitor.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating - non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5 V, V_{FB} = 0.8 V		900	1200	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V		3.6	10	µA
LOGIC THRESHOLD						
V_{EN}	EN high-level input voltage	EN	1.6			V
	EN low-level input voltage	EN			0.6	V
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, I_O = 10 mA, Eco-mode™ operation		771		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode operation	757	765	773	mV
		T_A = -40 to 85°C, V_O = 1.05 V, continuous mode operation(1)	751	765	779	mV
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V, T_A = 25°C		0	±0.15	µA
V_{REG5} OUTPUT						
V_{VREG5}	V_{REG5} output voltage	T_A = 25°C, 6.0 V < V_{IN} < 18 V, 0 < I_{VREG5} < 5 mA	5.2	5.5	5.7	V
V_{LNS}	Line regulation	6 V < V_{IN} < 18 V, I_{VREG5} = 5 mA			25	mV
V_{LDS}	Load regulation	0 mA < I_{VREG5} < 5 mA			100	mV
I_{VREG5}	Output current	V_{IN} = 6 V, V_{REG5} = 4.0 V, T_A = 25°C		60		mA
MOSFET						
$R_{DS(on)}$	High side switch resistance	25°C, V_{BST} - SW = 5.5 V		65		mΩ
	Low side switch resistance	25°C		36		mΩ
CURRENT LIMIT						
I_{OC}	Current limit	L out = 1.5 µH(1)	5.6	6.4	7.9	A

Functional Pin Description & Electrical Characteristics

D. TPS563200 (U102,U105, U106)

General Description

The TPS562200 and TPS563200 are simple, easy-to- use, 2 A and 3 A synchronous step-down (buck) converters in SOT-23 package.

The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

TPS562200 and TPS563200 operate in Advanced Eco-mode, which maintains high efficiency during light load operation. The devices are available in a 6- pin 1.6 x 2.9mm SOT (DDC) package, and specified from –40°C to 85°C of ambient temperature.

Features

- D-CAP2™ Mode Control with 650-kHz Switching Frequency
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- Integrated 68-mΩ and 39-mΩ FETs
- Advanced Eco-mode Pulse-skip
- Low Shutdown Current Less than 10 µA
- 1% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage

- Cycle-By-Cycle Hiccup Over-current Limit
- Non-latch OVP, UVLO and TSD Protections
- Fixed Soft Start: 1 ms

APPLICATIONS

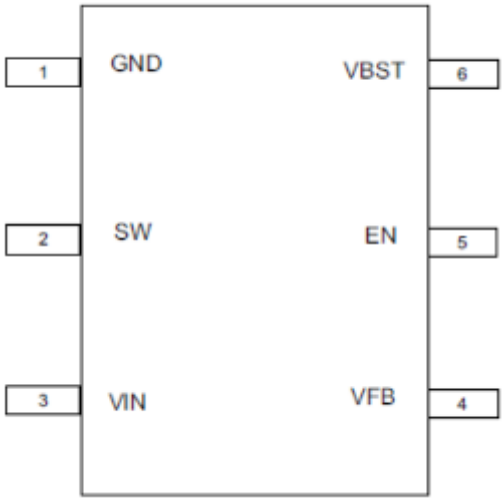
- Digital TV Power Supply
- High Definition Blu-ray Disc™ Players
- Networking Home Terminal
- Digital Set Top Box (STB)

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	17	V
V_I	Input voltage range	VBST	–0.1	23	V
		VBST (10 ns transient)	–0.1	26	
		VBST(vs SW)	–0.1	6	
		EN	–0.1	17	
		VFB	–0.1	5.5	
		SW	–1.8	17	
		SW (10 ns transient)	–3.5	20	
T_A	Operating free-air temperature		–40	85	°C

Table 3: Recommended operating conditions



Pin Description

Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect a 0.1µF capacitor between VBST and SW pins.

Electical Characteristics

over operating free-air temperature range, VIN = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{(VIN)}$	Operating – non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5V, V_{FB} = 0.8 V	TPS562200		230	330	µA
			TPS563200		190	290	
$I_{(VINSDN)}$	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V			3	10	µA
LOGIC THRESHOLD							
$V_{EN(H)}$	EN high-level input voltage	EN		1.6			V
$V_{EN(L)}$	EN low-level input voltage	EN				0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		225	450	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE							
$V_{FB(TH)}$	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, I_O = 10mA, Eco-mode™ operation			772		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode operation		758	765	772	mV
$I_{(VFB)}$	V_{FB} input current	V_{FB} = 0.8V, T_A = 25°C			0	±0.1	µA
MOSFET							
$R_{DS(on)h}$	High side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V	TPS562200		122		mΩ
			TPS563200		68		mΩ
$R_{DS(on)l}$	Low side switch resistance	T_A = 25°C	TPS562200		72		mΩ
			TPS563200		39		mΩ
CURRENT LIMIT							
I_{ocl}	Current limit [1]	DC current, V_{OUT} = 1.05 V, L_{OUT} = 2.2 µF	TPS562200	2.5	3.2	4.3	A
			TPS563200	3.5	4.2	5.3	A
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold [1]	Shutdown temperature			155		°C
		Hysteresis			35		
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
V_{OVP}	Output OVP threshold	OVP Detect (L > H)			125%		
V_{UVP}	Output Hiccup threshold	Hiccup detect (H > L)			65%		
t_{UVPEN}	Output Hiccup enable delay	Relative to soft-start time			x1.7		
UVLO							
UVLO	UVLO threshold	Wake up VIN voltage		3.45	3.75	4.05	V
		Hysteresis VIN voltage		0.13	0.32	0.55	

Pin functions and Electrical Characteristics

E. MP8774GQ-Z 12A QFN16 (U122)

DESCRIPTION

The MP8774 is a fully integrated high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. The MP8874 offers a very compact solution that achieves 12A of continuous output current with excellent load and line regulation over a wide input range. The MP8774 uses synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

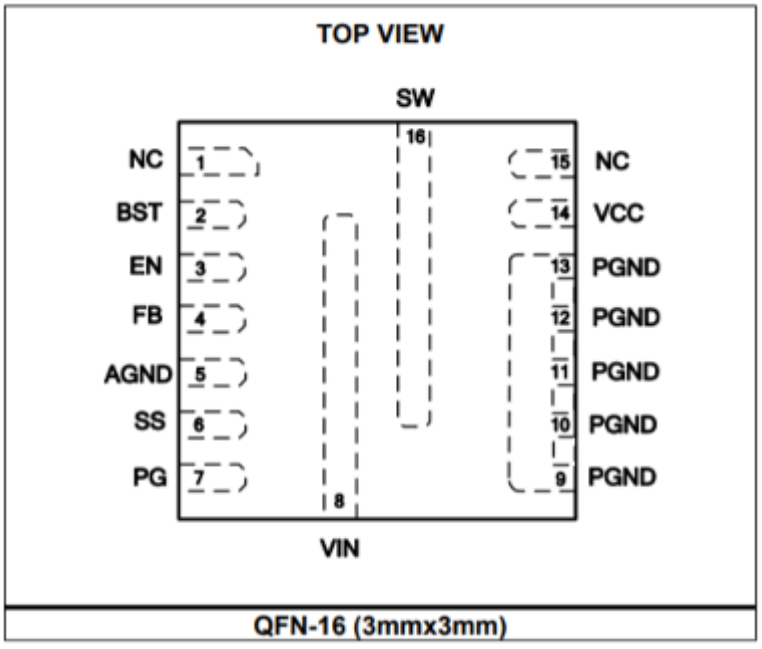
The MP8774 requires a minimal number of readily available, standard, external components and is available in a space-saving QFN-16 (3mmx3mm) package.

FEATURES

- Output Adjustable from 0.6V
- Wide 3V to 18V Operating Input Range
- 12A Output Current
- 16mΩ/5.5mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 100μA Quiescent Current
- High-Efficiency Synchronous Mode Operation
- Pre-Biased Start-Up
- Fixed 700kHz Switching Frequency
- External Programmable Soft Start-Up Time
- Enable (EN) and Power Good (PG) for Power Sequencing
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Security Cameras
- Portable Devices, XDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- General Purpose



Pin Assignment

PIN FUNCTIONS

Package Pin #	Name	Description
1, 15	NC	**No connection.** NC must be left floating.
2	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver. A BST resistor less than 4.7Ω is recommended.
3	EN	**Enable.** Pull EN high to enable the MP8774. When floating, EN is pulled down to GND and disabled by an internal 3.3MΩ resistor.
4	FB	**Feedback.** FB sets the output voltage when connected to the tap of an external resistor divider between output and GND.
5	AGND	**Signal ground.** AGND is not connected to the system ground internally. Ensure that AGND is connected to the system ground in the PCB layout.
6	SS	**Soft start.** Connect a capacitor across SS and GND to set the soft-start time to avoid inrush current at start-up.
7	PG	**Power good output.** The output of PG is an open drain. PG changes state if UVP, OCP, OTP, or OV occurs.
8	VIN	**Supply voltage.** The MP8774 operates from a 3 - 18V input rail. A capacitor (C1) is needed to decouple the input rail. Use a wide PCB trace to make the connection.
9 - 13	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. PGND requires careful consideration during the PCB layout. PGND is recommended to be connected to GND with coppers and vias.
14	VCC	**Internal bias supply output.** Decouple VCC with a 1μF capacitor. Place the VCC capacitor close to VCC and GND.
16	SW	**Switch output.** Connect SW with a wide PCB trace.

BLOCK DIAGRAM

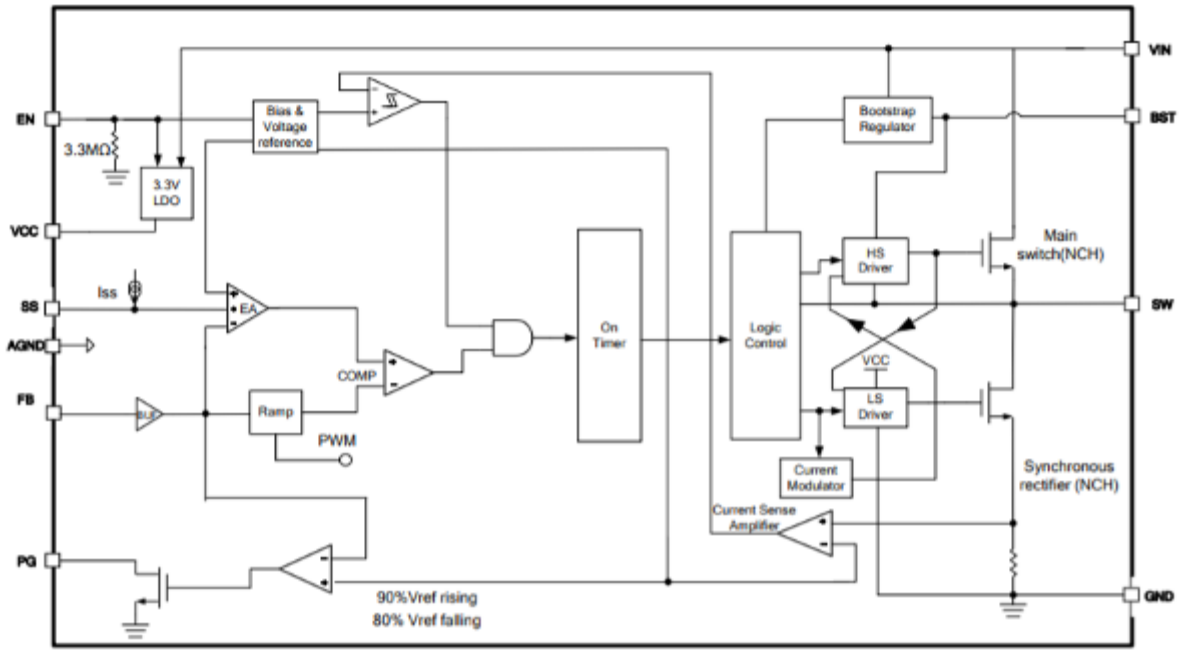


Figure 1: Functional Block Diagram

ELECTRICAL CHARACTERISTICS (6)

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		3		18	V
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			5	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		100	150	μA
MOSFET						
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 3.3V		16		mΩ
LS switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 3.3V		5.5		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 17V, T_J = 25°C			1	μA
Current Limit and ZCD						
Valley current limit	I_{LIMIT_VY}		12	14		A
Short hiccup duty cycle (7)	D_{HICCUP}			10		%
ZCD	I_{ZCD}			200		mA
Switching Frequency and Minimum On/Off Timer						
Switching frequency	Fs		600	700	800	kHz
Minimum on time (7)	$T_{On\ MIN}$			50		ns
Minimum off time (7)	$T_{Off\ MIN}$			100		ns
Reference and Soft Start						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start current	I_{SS_START}		4	6	8	μA
Enable and UVLO						
EN rising threshold	$V_{EN\ RISING}$		1.1	1.25	1.4	V
EN falling threshold	$V_{EN\ FALLING}$		0.9	1	1.1	V
EN pull-down resistor	R_{EN_PD}			1.2		MΩ
VCC						
VCC under-voltage lockout threshold rising	VCC_{Vth}		2.6	2.8	3	V
VCC under-voltage lockout threshold	VCC_{HYS}			350		mV
VCC regulator	V_{CC}			3.4		V
VCC load regulation	Reg_{VCC}	I_{CC} = 5mA		3		%

ELECTRICAL CHARACTERISTICS (6) *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good						
Power good UV rising threshold	$PGUV_{vth\_Hi}$		0.85	0.9	0.95	V_{FB}
Power good UV falling threshold	$PGUV_{vth\_Lo}$		0.75	0.80	0.85	V_{FB}
Power good OV rising threshold	$PGOV_{vth\_Hi}$		1.15	1.2	1.25	V_{FB}
Power good OV falling threshold	$PGOV_{vth\_Lo}$		1.05	1.1	1.15	V_{FB}
Power good delay	PG_{Td}	Both edge		50		μs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 5V			10	μA
Thermal Protection						
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SD-HYS}			20		°C

NOTES:

6) Guaranteed by over-temperature correlation, not tested in production.

7) Guaranteed by design and characterization test.

6. MICROCONTROLLER

MTK G31 (U108)

Description

The MT9685LAAJAC is MediaTek's latest SOC solution for UHD smart TV. Based on MediaTek's advanced technologies, the MT9685LAAJAC is integrated with the high-quality video processor which satisfies a variety of customer's requests for image quality to develop the state-of-the-art DTV system. The multi-core CPUs and GPUs deliver high performance for modern Linux and Android TVs. The up-to-date ARM and Mali architecture ensures the best software compatibility. Applications, such as HTML5, Java, Flash, and so on, are implemented with less efforts.

The MediaTek Professional PQ Engine includes all of MediaTek's most advanced color-tuning tools. MediaTek unique color processor with specially-designed color remapping systems assist System-developers to identify PQ characteristics of all the range of panel models quickly and easily. Moreover, MediaTek's innovated UltraClear video processor adopts the new technology for multi-frame video recovery so that contents or details can be restored perfectly and the noises or artifacts from broadcasting or internet can be eliminated.

The MT9685LAAJAC for DTV/MM/OTT applications into a single device, reducing the overall system BOM cost. With versatile peripheral connectivity ports, like HDMI, USB, Ethernet, CVBS, etc., the MT9685LAAJAC can serve as a high-quality media center in home entertainment field.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MT9685LAAJAC has an ultra-low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

Features

1 FEATURES

MT9685LAAJAC is a highly integrated smart TV solution, which supports LVDS/Vby1 output, DTV channel decoding, MPEG decoding, and security OS. MT9685LAAJAC serves full functions of multi-media centers with a high performance CPU, GPU, and AV CODEC/security engines.

Key features includes:

1. *Combo Front-End Demodulators*
2. *Advanced Multi-Core CPU and 3D GPU*
3. *3D Formatter Engine*
4. *Multi-Standard A/V Format Decoder*
5. *MediaTek High Performance Video Processor and MediaTek Professional PQ Engine*
6. *Home Theater Sound Processor*
7. *Internet and Variety of Connectivity Support*
8. *Peripheral and Power Management*
9. *Robust and Efficient Security Engine*
10. *Full Multi-Media Decoders Including HEVC Decoder Supporting up to UHD/60fps Resolution*

- High Performance Micro-processor
  - ARM Advanced Multi-Core Cortex CPU
  - 32KB/32KB I/D cache
  - 512KB L3 cache
  - Supports Neon instruction sets
- 3D Graphic GPU
  - ARM Advanced Multi-Core Mali GPU
  - Vulkan 1.1
  - Supports OpenGL ES 3.2/2.0/1.1
  - Supports OpenCL 2.0
  - Supports DirectX 11 FL9_3
  - Supports rendering size up to UHD
- Transport Stream De-multiplexer
  - Supports two parallel and one serial TS inputs interfaces, with or without sync signal
  - Supports one of TS PAD is programmable TS input/output
  - Supports external demodulators
  - TS data rate is 140Mbit/s for serial and 56MByte/s for parallel
  - 128 general purpose PID filters and 128 section filters for all transport stream de-multiplexer
  - Supports additional audio/video/PCR filters
  - Supports time-shift
  - Supports 3DES/DES and AES encryption/decryption
- MPEG-2 Video Decoder
  - ISO/IEC 11172-2 MPEG-1 video format decoding
  - ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
  - Supports resolution up to HDTV (1080p60, 1080i, 720p) and SDTV
  - Supports dual stream decoding for 3D content
  - Supports for FHDp60 2x fast forwarding playback
- MPEG-4 Video Decoder
  - ISO/IEC 14496-2 MPEG-4 ASP video decoding up to HD level
  - Supports resolutions up to HDTV (1080p@60fps)
  - Supports FLV version1 video format decoding
  - Supports dual stream decoding for 3D content

- H.264 Decoder
  - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 5.2) video decoding
  - Supports resolution up to 4096x2160@60fps
  - Supports bitrate up to 135Mbps
  - Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
  - Supports SVAF 2ES (for Dual Decode)
  - Supports MVC 3D decoding upto 1080p@60fps
- VP8 Decoder
  - Supports Google VP8 decoder
  - Supports resolution up to 1920x1080@60fps
  - Supports maximum bitrate upto 50Mbps
- VP9 Decoder
  - Supports Google VP9 decoder
  - Supports 4:2:0 subsampling and 8bit/10bit color depth
  - Supports max resolution and frame rate 4096x2160@60fps
  - Supports max bitrate upto 100Mbps
- AV1 Video Decoder
  - Supports AV1 video decoding
  - Supports Main profile, level 5.1
  - Supports 8-bit/10-bit color depth
  - Supports resolution up to 4096x2304@60fps
  - Supports max bitrate up to 100Mbps
- HEVC (H.265) Decoder
  - Supports HEVC/H.265 video decoding
  - Supports Main/Main-10 profile, and Scalable Main/Scalable Main-10 profile, level 5.1, high tier
  - Supports 8-bit/10-bit color depth
  - Supports resolution up to 4096x2160@60fps, or 4096x2160@60fps+1920x1080@60fps for Dolby Vision
  - Supports max bitrate upto 100Mbps
- H.264 Encoder[Optional]
  - Supports H.264 encoding, Main Profile, level 4.1
  - Maximum output frame-rate/resolution: 1920x1080@30fps, 1280x720@60fps
  - Supports MVs: 16x16, 16x8, 8x16, 8x4, 4x8, 4x4
  - Supports up to quarter-pel
  - Supports up to two reference frames
- Hardware JPEG Decoder
  - Supports upto 1920x1080@30fps, 1280x720@60fps
  - Supports formats: 422/411/420/444/422T
  - Supports scaling down ratios: 1/2x1/2, 1/4x1/4, 1/8x1/8
  - Supports both color and grayscale pictures
  - Supports sequential mode, single scan
  - Supports programmable Region of Interest (ROI)
  - Following the file header scan the hardware decoder fully handles the decode process
- VC-1 Video Decoder
  - Supports SMPTE-421M (VC1 video) decoding up to AP@L3 (2048x1024p60)
  - Supports dual stream decoding for 3D content
- NTSC/PAL/SECAM Video Decoder
  - Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
  - Automatic standard detection
  - Motion adaptive 3D comb filter
  - Supports CVBS & Y/C S-video inputs
  - Supports V-chip

- Multi-Standard TV Sound Processor
  - Supports BTSC/A2 demodulation
  - Supports FM/AM demodulation
  - Supports MTS Mode Mono/Stereo/SAP in BTSC mode
  - Supports Mono/Stereo/Dual in A2 mode
  - Built-in audio sampling rate conversion (SRC)
  - Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
  - Advanced sound processing options available, for example: Dolby[1], DTS[2], DBX-TV[3]
  - Supports digital audio format : MPEG-1, MPEG-2 (Layer I/II), MP3, AAC-LC, HE-AAC, WMA, WMA9 Pro
  - Supports Multi-stream programs: Dolby MS12-B Optional, Dolby MS12-D Optional, Dolby MS12-Y Optional, Dolby MS12-Z Optional, and DTS M6 Optional, DTS M6 multistream decoder/encoder
  - Supports Audio Description
  - Supports MPEG audio encoding
  - Supports time-shifting PVR
  - Supports programmable delay for audio/video synchronization
- Audio Interface
  - One L/R audio line-input
  - One L/R output for main speaker or additional line-output
  - Supports stereo headphone driver
  - I²S digital audio output and input
  - S/PDIF digital audio output and input
  - Supports HDMI receiver ARC function
  - Supports PDM input for 2/4 channels digital microphone
- Analog RGB Compliant Input Ports
  - Two analog ports support up to 1080P
  - Supports PC RGB input up to SXGA@75Hz
  - Supports HDTV RGB/YPbPr/YCbCr
  - Supports Composite Sync and SOG Sync-on-Green
  - Automatic color calibration
- Analog RGB Auto-Configuration & Detection
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset and gain configuration
  - Sync Detection for H/V Sync

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[1] Trademark of Dolby Laboratories

[2] Trademark of DTS, Inc.

Optional Please see Ordering Guide for details

[3] Trademark of DBX-TV, Inc.

- DVI/HDCP/HDMI Compliant Input Ports
  - Four HDMI/DVI input ports
  - HDMI 2.0b/1.4b Compliant
  - HDMI 2.1
    - Max bit rate upto 6Gbps in TMDS
    - VRR and Dynamic HDR EM packet
  - MediaTek iSwitch for fast HDMI switching
  - HDCP 2.2/1.4 Compliant
  - Supports HDMI CEC
  - Supports HDMI ARC/eARC TX
  - Robust receiver with excellent long-cable support
- MediaTek High Performance Video Processor
  - Video Processing Engine
    - Supports up to 4K UHD@60p
    - 10/12-bit Internal Data Processing
    - Arbitrary Frame Rate Conversion
  - Video Care Technology
    - Video Line Broken Artifact Detection and Removal
    - Video Detection & Repairing Technology for Lousy Inputs such as Internet Streaming
  - Fully Programmable Multi-Function Scaling Engine
    - High-Quality Filters with Programmable Parameter
    - An advanced Zoom Algorithm providing Aliasing/Ringing Suppression
    - Nonlinear Video Scaling supports various modes including Panorama
    - Supports Dynamic Scaling for VC-1
    - Fully Programmable Zoom Ratios for Up/Down Scaling
    - Independent Horizontal and Vertical Zoom
  - Deinterlacer
    - Advanced Motion Compensated Video Deinterlacing with Motion Object Stabilizer
    - Motion De-Flickering
    - Motion Adaptive Deinterlacer
    - Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal
    - Automatic 3:2/2:2/M:N Pull-Down Detection and Recovery
  - MediaTek Genuine 3D
    - Supports Mandatory 3D Format
  - Motion Frame Rate Conversion
    - Supports Frame Repeat Frame Rate Conversion
    - Supports 4K Motion Compensated Frame Rate Conversion
    - Advanced Halo Reduction
    - Automatic Film-Mode Detection/Film Judder Cancellation
    - Search Range: Big H and V search range to handle fast motion
    - Supports Logo Detection and Protection
    - Supports Small Object Detection and Protection
    - Supports LetterBox
  - Backlight Technology
    - Supports Direct and Edge Types Local Dimming
    - Programmable Light Spread Profile
    - Content Adaptive LCD Backlight Control
  - High Dynamic Range
    - Supports SMPTE ST-2084/ST-2086
    - Supports ARIB STD-B67(Hybrid Log Gamma)/BT.2100
    - Supports 2094-40 (HDR10 plus)optional
    - Supports ITU-R BT.2100
    - Ultra HD Premium Ready
    - Dolby Vision
  - Response Time Compensation
    - Supports Overdrive Technology

- MediaTek Professional PQ Engine
  - UltraClear
    - MPEG Artifact Removal
      - Advanced Adaptive Block Noise Reduction
      - Advanced Mosquito Noise Cancellation
      - Supports DCR Engine
    - UltraClear Noise Reduction
      - Ultimate 3D Motion-Compensated Temporal Filtering
      - Auto Noise Estimation
    - 3D Noise Reduction
      - 3D Temporal Noise Reduction for Lousy Air/Cable Input
  - S-Powers
    - Video Enhancement Processor
      - Advanced 3D Independent Multi-Band Control Sharpness Technology
      - Advanced Video Enhancement Algorithm provides Aliasing/Ringing Suppression
      - Advanced Chroma Transient Improvement
      - Supports Luma Transient Improvement
    - Super Resolution
      - Local Detail Enhancement
      - SuperiorClear Multi-Directional Anti-Aliasing and Jagged Compensation Technology
      - SuperiorClear Enhance Management
  - MACE
    - MediaTek Advanced Color Engine
      - MediaTek Graffito Color Manager
      - Color Stain Removal Technology
    - Standard Color Format and Processing
      - Fully Programmable Input/Output CSC
      - BT601, BT709, BT2020 (CL/NCL)
      - xvYCC601, xvYCC709
      - AdobeRGB, AdobeYCC601
      - sRGB, sYCC601
      - Fully Programmable 12-bit RGB Gamma
    - Gamut Mapping
      - Nonlinear/Linear RGB Domain Gamut Mapping
      - Supports 2D Gamut Mapping
      - Supports 3D Gamut Mapping
  - Luce
    - Contrast Enhancement
      - Real-Time Content Adaptive Contrast Enhancement with Chroma Compensated
      - Ultra Contrast Dimming
    - SDR to HDR

- Output Interface
  - Single/Dual link 8-bit/10-bit LVDS output
  - Supports panel resolution up to Full HD 1920x1080@60Hz (LVDS 2ch)
  - 8-lane 8-bit/10-bit Vby1 output (configurable width: 2/4/8 lane)
  - Supports panel resolution up to Ultra HD @60Hz (Vby1 8 lane)
  - Supports OSD bypass to MTK FRC 120Hz/240Hz chip[Optional]
  - Supports TCON:EPI interface, panel resolution up to Ultra HD@60Hz
  - Supports TCON:CMPI interface, panel resolution up to Ultra HD@60Hz
  - Supports TCON:ISP interface, panel resolution up to Ultra HD@60Hz
  - Supports TCON:CHPI interface, panel resolution up to Ultra HD@60Hz
  - Supports TCON:CEDS interface, panel resolution up to Ultra HD@60Hz
  - Supports TCON:CSPI interface, panel resolution up to Ultra HD@60Hz
  - Supports TTL output, update to 1920x1080@60Hz
  - Supports programmable timing controller
  - Supports dithering options
  - Spread spectrum output frequency for EMI suppression
  - Supports 60Hz 3D polarizd panel (line interleave)
  - Supports Cinema output mode
- CVBS Video Encoder
  - Supports all NTSC/PAL TV Standard
  - Stand-alone scaling engine (no vertical scaling up)
  - Programmable Hue, Contract, Brightness
  - Supports WSS output
- CVBS Video Output
  - Allows CVBS output of digital content to SCART
- 2D Graphics Engine
  - Hardware Graphics Engine for responsive interactive applications
  - Supports line draw, rectangle draw/fill and text draw
  - Supports BitBlt, Stretch BitBlt, Italic Bitblt, Mirror BitBlt and Rotate BitBlt
  - Supports alpha-blending operation
  - Supports source/destination color key and alpha key
  - Supports dither
  - Supports color format conversion and format transformation
  - Raster Operation (ROP)
  - Supports DFB and Porter-Duff operation
- VIF Demodulator
  - Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards
  - Supports low IF architecture
  - Audio/Video internal dual-path processor
  - Locking range improvement

- ATSC/QAM Demodulator
  - ATSC A/53 compliant 8VSB
  - ITU-T J.83 Annex B, SCTE DVS-031 compliant 64/256QAM receiver
  - 2010 - A74 compliant
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - Integrated deinterleaver RAM for Level 1 J =1 and Level 2 J= 1,2,3.4
  - Supports LIF interfaces
- DVB-C Demodulator
  - Compliant with ITU J.83 Annex A/C DVB-C (EN 300 429)
  - Supports 1-7.2 M Baud symbol rate
  - Automatic blind channel scan (constellation and symbol rate)
  - Supports LIF interfaces
  - IIS performance improvement
- DVB-T Demodulator
  - Compliant with DVB-T (ETSI EN 300 744)
  - Nordig 2.2.2, D-book 7.0 compliant
  - Accept low IF inputs in 6, 7, 8MHz channel bandwidths
  - Supports all guard intervals (1/32 to 1/4)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM)
  - Ultra fast automatic blind UHF/VHF channel scan
  - Optimized for SFN channels with pre/post-cursive echoes inside/outside the guard
  - Phase-Noise suppression
  - Impulse-Noise suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - CNR performance improvement
  - Outside-GI performance improvement
- DVB-T2 Demodulator
  - Compliant with DVB-T2 (ETSI EN 302 755) v1.3.1, T2-base & T2-Lite profile
  - Nordig Unified 2.2.2, D-Book 7.0 compliant
  - Supports all guard intervals (1/128 to 1/4)
  - Supports all FFT modes from 1K to 32K
  - Supports all long and short block code rates (1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 2/5, 1/3)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM, 256-QAM)
  - Transmit diversity (MISO) support
  - Supports all scattered pilot patterns (PP1 to PP8)
  - Supports rotated and non-rotated constellations
  - Supports single and multiple PLPs
  - Accept low IF inputs in 1.7, 5, 6, 7, 8MHz channel bandwidths
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - Outside GI improvement
  - Locking time improvement
- DVB-S Demodulator
  - Compliant with DVB-S (ETSI EN 300 421)
  - Data Rate: 1-70 Msps
  - Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
  - Carrier frequency acquisition range: 5MHz
  - Fast automatic blind scan of symbol rates and carrier frequencies
  - Equalizer compensates for channel impairment
  - DiSEqC™ 2.0 compatible with LNB controller
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset

- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors
- Improved CNR performance

■ DVB-S2 Demodulator

- Compliant with DVB-S2 (ETSI EN 302 307)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 16APSK, 1-57 Msps for 32APSK
- Constellations: QPSK , 8PSK , 16APSK and 32APSK
  - QPSK Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
  - 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10
  - 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
  - 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9, 9/10
- Supports CCM and VCM
- Supports Single Transport Stream and Multiple Transport Streams
- Roll-off factors for pulse shaping: 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqC™ 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

■ DVB-S2X Demodulator

- Compliant with DVB-S2 Extensions (ETSI EN 302 307-2, Broadcast services except for Channel Bonding)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 8APSK-L, 16APSK, 16APSK-L, 1-57 Msps for 32APSK, and 32APSK-L
- Constellations: QPSK , 8PSK, 8APSK-L, 16APSK, 16APSK-L, 32APSK, and 32APSK-L
  - QPSK Code Rates: 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 13/45, 9/20, 11/20
  - 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10, 23/36, 25/36, 13/18
  - 8APSK-L Code Rates: 5/9, 26/45
  - 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 26/45, 3/5, 28/45, 23/36, 25/36, 13/18, 7/9, 77/90
  - 16APSK-L Code Rates: 5/9, 8/15, 1/2, 3/5, 2/3
  - 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9, 9/10, 32/45, 11/15, 7/9
  - 32APSK-L Code Rates: 2/3

- Supports CCM and VCM
- Supports Single Transport Stream and Multiple Transport Streams
- Roll-off factors for pulse shaping: 0.05, 0.1, 0.15, 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqC™ 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

■ Connectivity

- Three USB 2.0 host ports
- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
- Embedded 10/100 Ethernet PHY
- Supports Ethernet Wake-On-Lan

■ Miscellaneous

- DRAM interface supports DDR3
- Supports PVR
- Parallel interface for external parallel eMMC flash and NAND flash support
- Power control module with ultra low power MCU available in standby mode
- 542-ball BGA package

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}		TBD		V
1.5V Supply Voltages (DDR3)	V_{VDD_15}		TBD		V
Core Supply Voltages	V_{VDD_core}		TBD		V
CPU Supply Voltages	V_{VDD_cpu}		TBD		V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Recommended operating condition

7. 8 GB EMMC

SAMSUNG EMMC 8GB KLM8G1GETF-B041 BGA153 (U128)

Description

SAMSUNG eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a sim-ple read and write to memory using MMC protocol v5.1 which is a industry standard. eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply voltage (VDD or VCCQ) is supported for the MMC controller. SAMSUNG eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance. There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market. The embedded flash management software or FTL(Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

Key Features

- Embedded MultiMediaCard Ver. 5.1 compatible.
- SAMSUNG eMMC supports features of eMMC5.1 which are defined in JEDEC Standard

- Major Supported Features : HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types

- Non-supported Features : Large Sector Size (4KB)

- Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems)
- Data bus width : 1bit (Default), 4bit and 8bit
- MMC I/F Clock Frequency : 0 ~ 200MHz
  MMC I/F Boot Frequency : 0 ~ 52MHz
- Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)

Power : Interface power →VCCQ(1.70V ~ 1.95V), Memory power → VCC(2.7V~ 3.6V)

Item	Min	Max	Unit
V_{CCQ}	1.70	1.95	V
V_{CC}	2.7	3.6	V
V_{SS}	-0.5	0.5	V

Table: Supply Voltage

8. USB INTERFACE

USB POWER SWITCH ADJ SAFE TPS25221 SOT23-6 (U117-U109)

1 Features

- 2.5-V to 5.5-V $V_{OPERATING}$
- Pin-to-Pin with TI Switch Portfolio
- 2-A I_{CONT_MAX}
- 0.277-A to 2.7-A Adjustable I_{LIMIT} (±10% at 2.7 A)
- 70-mΩ (typical) R_{ON}
- 2-µs Short Circuit Response
- 8-ms Fault Reporting Deglitch
- Reverse Current Blocking (when disabled)
- Built-In Soft Start
- UL 60950 and UL 62368 Recognition Pending
- 15-kV ESD Protection per IEC 61000-4-2 (with external capacitance)

2 Applications

- USB Ports/Hubs, Laptops, Desktops
- High-Definition Digital TVs
- Set Top Boxes
- Optical Socket Protection

3 Description

The TPS25221 is intended for applications such as USB where heavy capacitive loads and short circuits may be encountered. The programmable current-limit threshold maybe set between 277 mA and 2.7 A (typical) using an external resistor. Current-limit accuracy as tight as ±10% can be achieved at the higher current-limit settings. The power-switch rise and fall times are controlled to minimize current surges during turn on and turn off.

The TPS25221 limits output current to the programmed level when the output load attempts to exceeds the current-limit threshold. The $\overline{FAULT}$ output asserts low during overcurrent conditions.

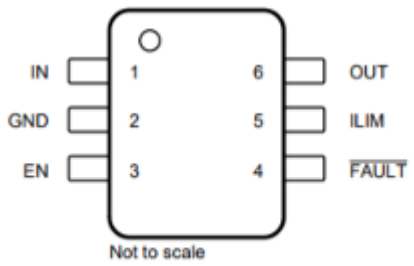
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS25221	SOT-23 (6)	2.90 mm x 1.60 mm
	WSON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

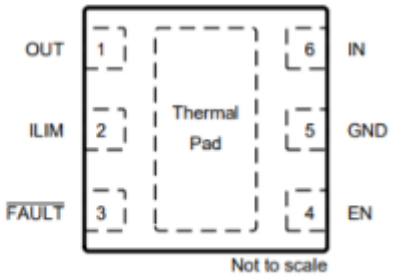
Pin Configuration and Functions

DBV PACKAGE
SOT-23 6-Pin
Top View



Not to scale

DRV PACKAGE
WSON 6-Pin
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	WSON		
IN	1	6	I	Input voltage and power switch drain; connect a 0.1 µF or greater ceramic capacitor from IN to GND close to IC
GND	2	5	--	Ground connection
EN	3	4	I	Enable input, logic high/low turns on power switch
$\overline{FAULT}$	4	3	O	Active-low open-drain output, asserted during over-current, or over-temperature conditions
ILIM	5	2	O	External resistor used to set current limit threshold
OUT	6	1	O	Power switch output, connect to load
Thermal Pad	--	PAD	--	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect thermal pad to GND pin externally.

7.5 Electrical Characteristics

over recommended operating conditions, $V_{EN} = V_{IN}$, R_{FAULT} = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	Static drain-source on-state resistance	DBV package, T_J = 25°C			70	80	mΩ
		DBV package, –40°C ≤T_J ≤125°C				110	
		DRV package, T_J = 25°C			70	92	
		DRV package, –40°C ≤T_J ≤125°C				122	
t_r	Rise time, output	V_{IN} = 5.5 V	C_L = 1 µF, R_L = 100 Ω, (see 図 1)		0.55	0.95	ms
		V_{IN} = 2.5 V			0.35	0.62	
t_f	Fall time, output	V_{IN} = 5.5 V			0.24	0.3	
		V_{IN} = 2.5 V			0.22	0.28	
ENABLE INPUT EN OR $\overline{EN}$							
	Enable pin turn on/off threshold			0.8		1.6	V
I_{EN}	Input current	V_{EN} = 0 V or 5.5 V		-0.5	0	0.5	µA
t_{on}	Turnon time	C_L = 1 µF, R_L = 100 Ω, (see 図 2)				3	ms
t_{off}	Turnoff time	C_L = 1 µF, R_L = 100 Ω, (see 図 2)				0.7	ms
CURRENT LIMIT							
I_{OS}	Current-limit threshold (Maximum DC output current I_{OUT} delivered to load) and Short-circuit current, OUT connected to GND	R_{ILIM} = 20 kΩ	T_J = 25°C	2585	2720	2850	mA
			–40°C ≤T_J ≤125°C	2560		2880	
		R_{ILIM} = 30 kΩ	T_J = 25°C	1710	1820	1930	
			–40°C ≤T_J ≤125°C	1700		1945	
		R_{ILIM} = 80 kΩ	T_J = 25°C	630	690	755	
			–40°C ≤T_J ≤125°C	610		790	
		R_{ILIM} = 210 kΩ	T_J = 25°C	220	275	330	
			–40°C ≤T_J ≤125°C	210		370	
t_{IOS}	Response time to short circuit	V_{IN} = 5 V (see 図 4)			1.5		µs
SUPPLY CURRENT							
I_{SD}	Supply current, switch disable	V_{IN} = 5.5 V, No load on OUT, V_{EN} = 0 V,R_{ILIM} = 20 kΩ			0.02	0.5	µA
I_{SE}	Supply current, switch enable	V_{IN} = 5.5 V, No load on OUT ,R_{ILIM} = 20 kΩ			75	90	µA
UNDERVOLTAGE LOCKOUT							
UVLO	Low-level input voltage, IN	V_{IN} rising			2.37	2.47	V
	Hysteresis, IN	T_J = 25 °C			45		mV
$\overline{FAULT}$ FLAG							
V_{OL}	Output low voltage, $\overline{FAULT}$	$I_{/FAULT}$ = 1 mA				180	mV
	Off-state leakage	$V_{/FAULT}$ = 5.5 V				0.5	µA
	$\overline{FAULT}$ deglitch	$\overline{FAULT}$ assertion or de-assertion due to overcurrent condition		6	8	12	ms
THERMAL SHUTDOWN							
	Thermal shutdown threshold				165		°C
	Thermal shutdown threshold in current-limit				145		°C
	Hysteresis				20		°C

9. CI INTERFACE

17MB185 Digital CI ve Smart Card Interface Block diagram:

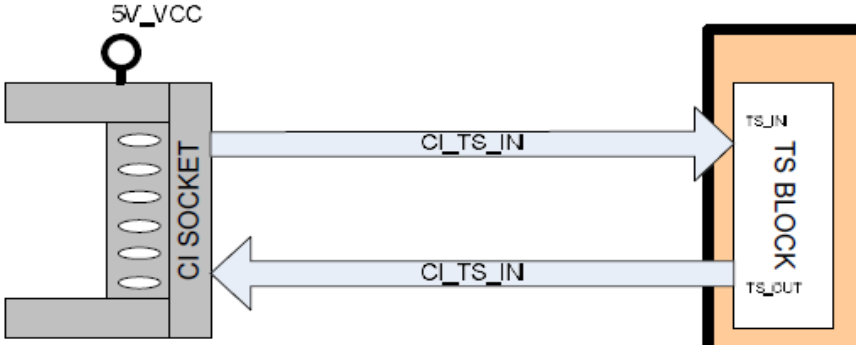


Figure: CI interface

10. SOFTWARE UPDATE

MAIN SOFTWARE UPDATE

In 17MB185 project, please follow software update procedure:

Method-1

1. Copy MstarUpgrade.bin to USB stick (root directory, FAT32)
2. Enter M-Boot console first (Long press "ENTER" key on Tera Term Console when your device reboot then do AC On)
3. Plug the USB stick to your target board
4. Execute "custar" in M-Boot console to perform upgrading

Method-2

1. Copy upgrade_loader.pkg to root folder of USB stick (or copy upgrade_loader_no_tvcertificate.pkg if you don't want to erase keys, credentials, etc.)
2. Insert USB disk to one of the USB ports on your TV
3. Power on TV and wait until you see the bootlogo
4. You should see logs like below

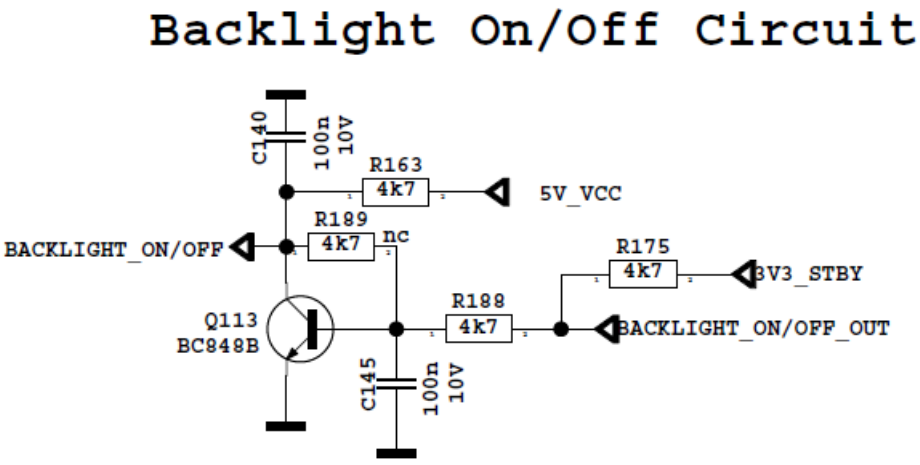
11. TROUBLESHOOTING

A. NO BACKLIGHT PROBLEM

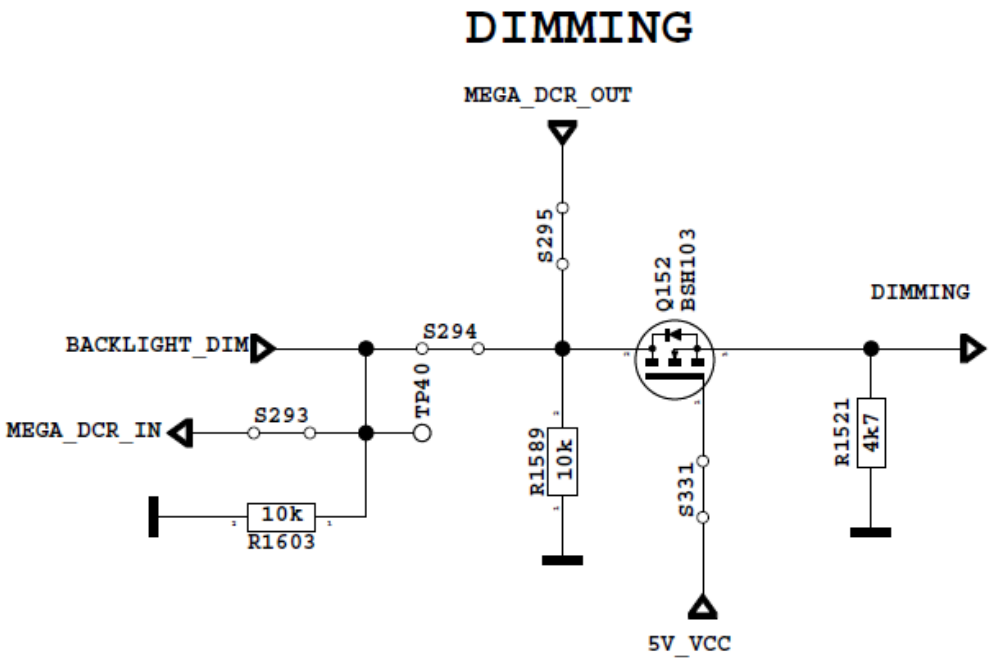
Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply, stby on/off pin

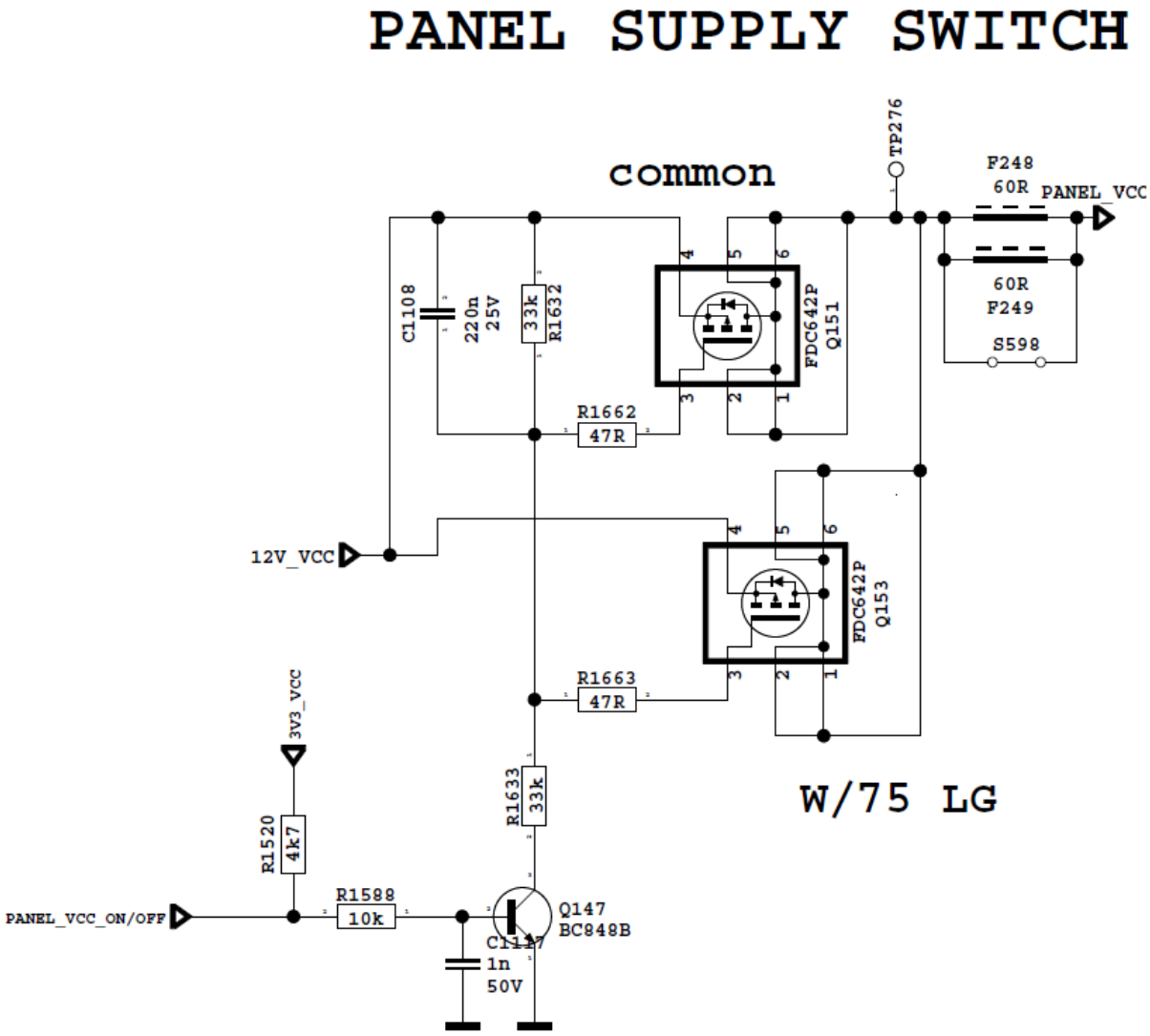
BACKLIGHT_ON/OFF pin should be high when the backlight is ON. Collector pin of Q113 must be low when the backlight is OFF. If it is a problem, please check Q181. Also it can be tested in TP500 or Pin5 of CN2 in main board. Please also check panel cables.



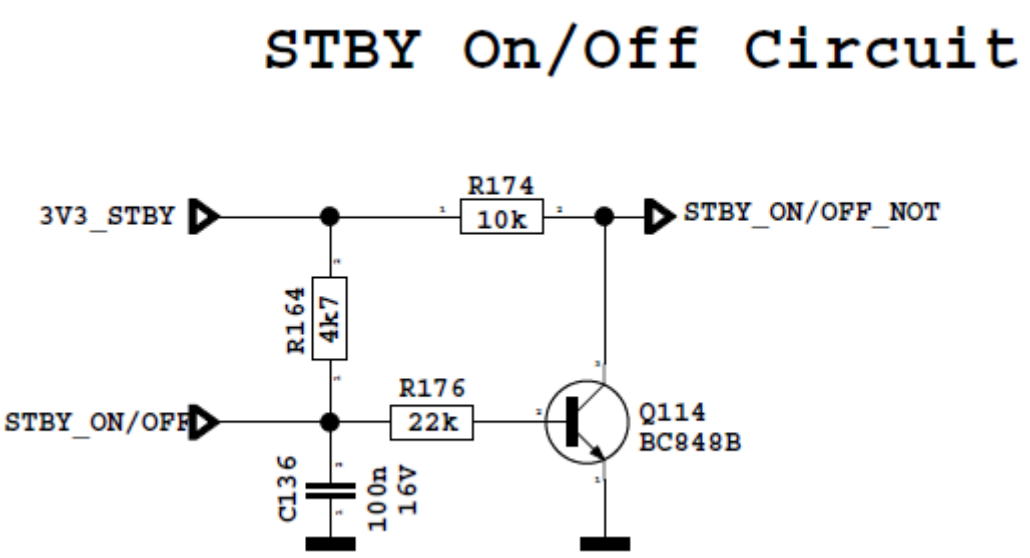
Dimming pin should be high or square wave in open position. If it is low, please check S294 for MTK side. It also can be checked at TP499. Please also check panel or power cables and connectors.



Panel power supply should be in panel specs. Please check Q151, shown below; also it can be checked TP276.



STBY_ON/OFF should be low for TV on condition, please check Q114's collector.

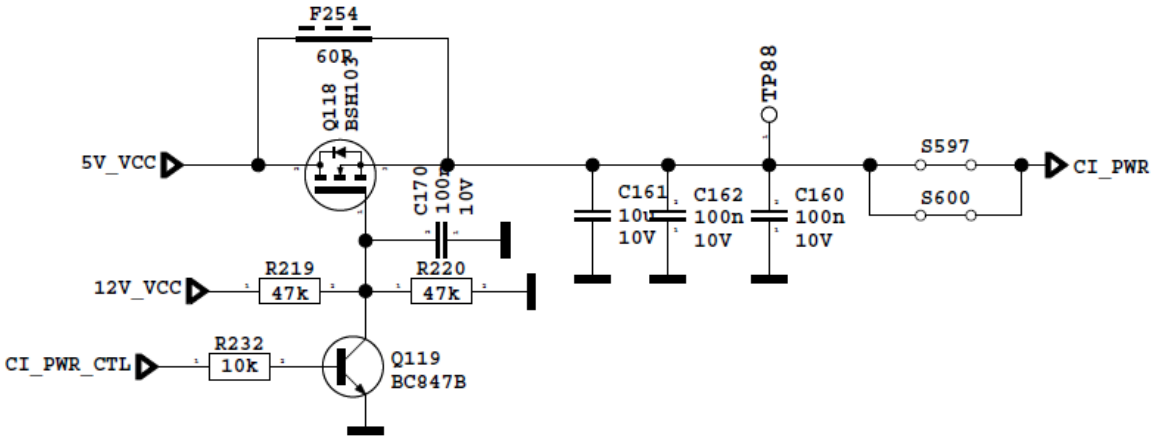


B. CI MODULE PROBLEM

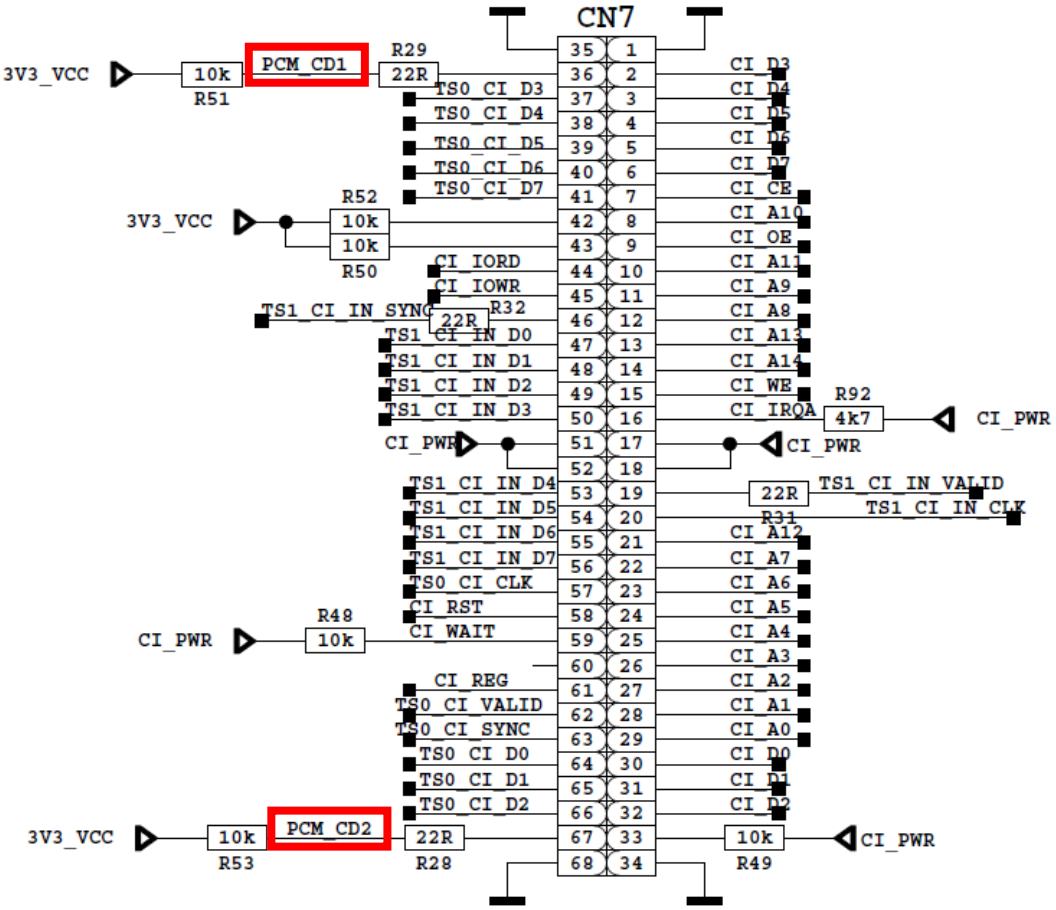
Problem: CI is not working when CI module inserted.

Possible causes: Supply, supply control pin, detects pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTRL, this pin should be low.



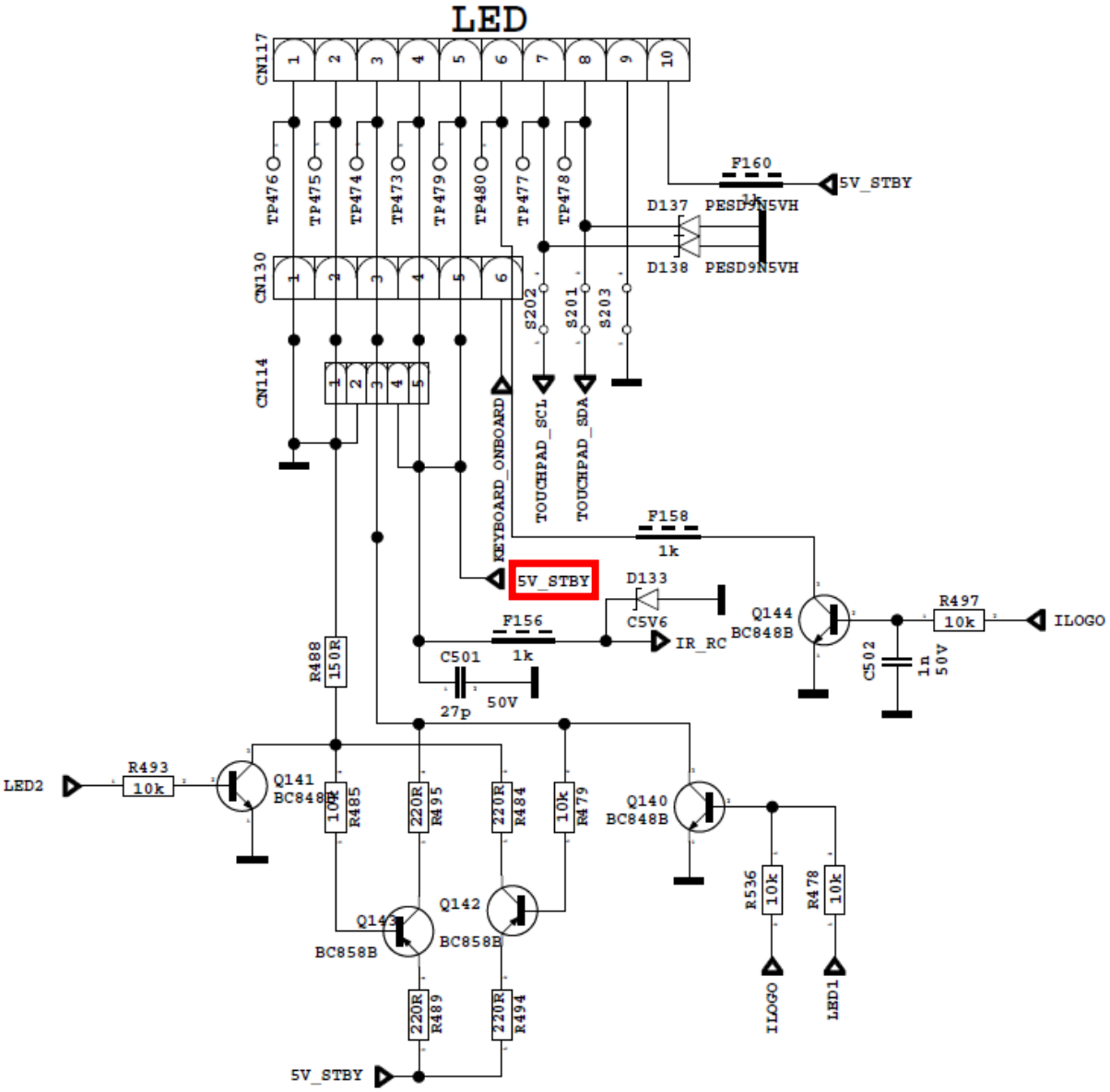
- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.


CN7
3V3_VCC
10k
R51
PCM_CD1
R29
22R
TS0_CI_D3
TS0_CI_D4
TS0_CI_D5
TS0_CI_D6
TS0_CI_D7
R52
10k
10k
R50
3V3_VCC
CI_IORD
CI_IOWR
TS1_CI_IN_SYNC
R32
22R
TS1_CI_IN_D0
TS1_CI_IN_D1
TS1_CI_IN_D2
TS1_CI_IN_D3
CI_PWR
TS1_CI_IN_D4
TS1_CI_IN_D5
TS1_CI_IN_D6
TS1_CI_IN_D7
TS0_CI_CLK
CI_RST
CI_WAIT
R48
10k
CI_PWR
CI_REG
TS0_CI_VALID
TS0_CI_SYNC
TS0_CI_D0
TS0_CI_D1
TS0_CI_D2
3V3_VCC
10k
R53
PCM_CD2
22R
R28
CI_D3
CI_D4
CI_D5
CI_D6
CI_D7
CI_CE
CI_A10
CI_OE
CI_A11
CI_A9
CI_A8
CI_A13
CI_A14
CI_WE
CI_IRQA
R92
4k7
CI_PWR
CI_PWR
22R
TS1_CI_IN_VALID
TS1_CI_IN_CLK
R31
CI_A12
CI_A7
CI_A6
CI_A5
CI_A4
CI_A3
CI_A2
CI_A1
CI_A0
CI_D0
CI_D1
CI_D2
10k
R49
CI_PWR

C. IR PROBLEM

Problem: LED or IR not working

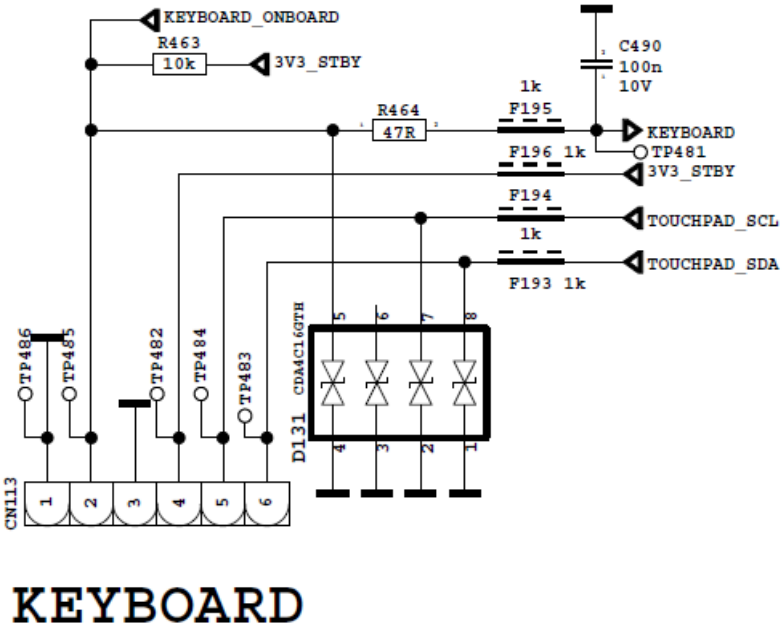
Check LED card supply on 17MB185 chasis.



D. KEYPAD TOUCHPAD PROBLEMS

Problem: Keypad or Touchpad is not working

Check keypad supply on 17MB185.

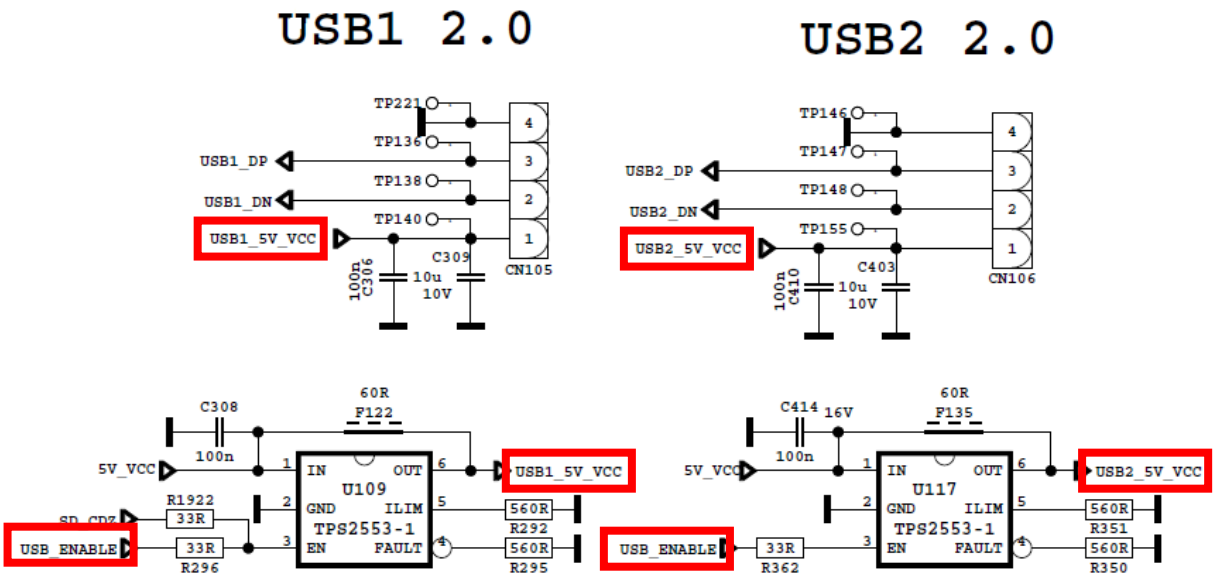


E. USB PROBLEMS

Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

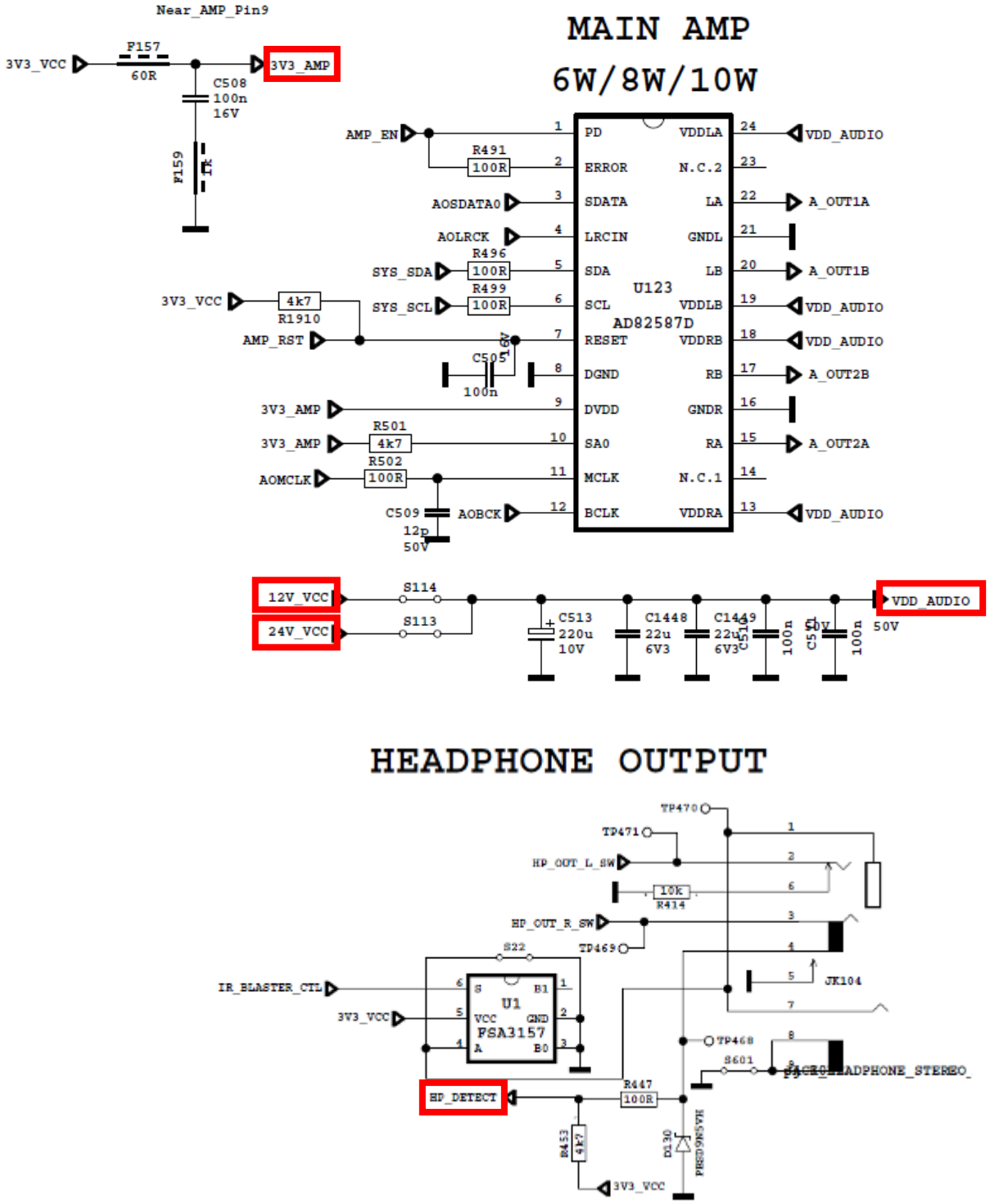
USB Control is optional, so U109 and U117 may not be added. Check supply voltages only.



F. NO SOUND PROBLEM

Problem: No audio at main TV speaker outputs.

Check supply voltages of 24V_VCC, VDD_AUDIO and 3V3_AMP with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3V.



G. STANDBY ON/OFF PROBLEM

Problem: Device cannot boot, TV hangs in standby mode.

There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm program. These printouts may give a clue about the problem. You can use VGA for Teraterm program connection.

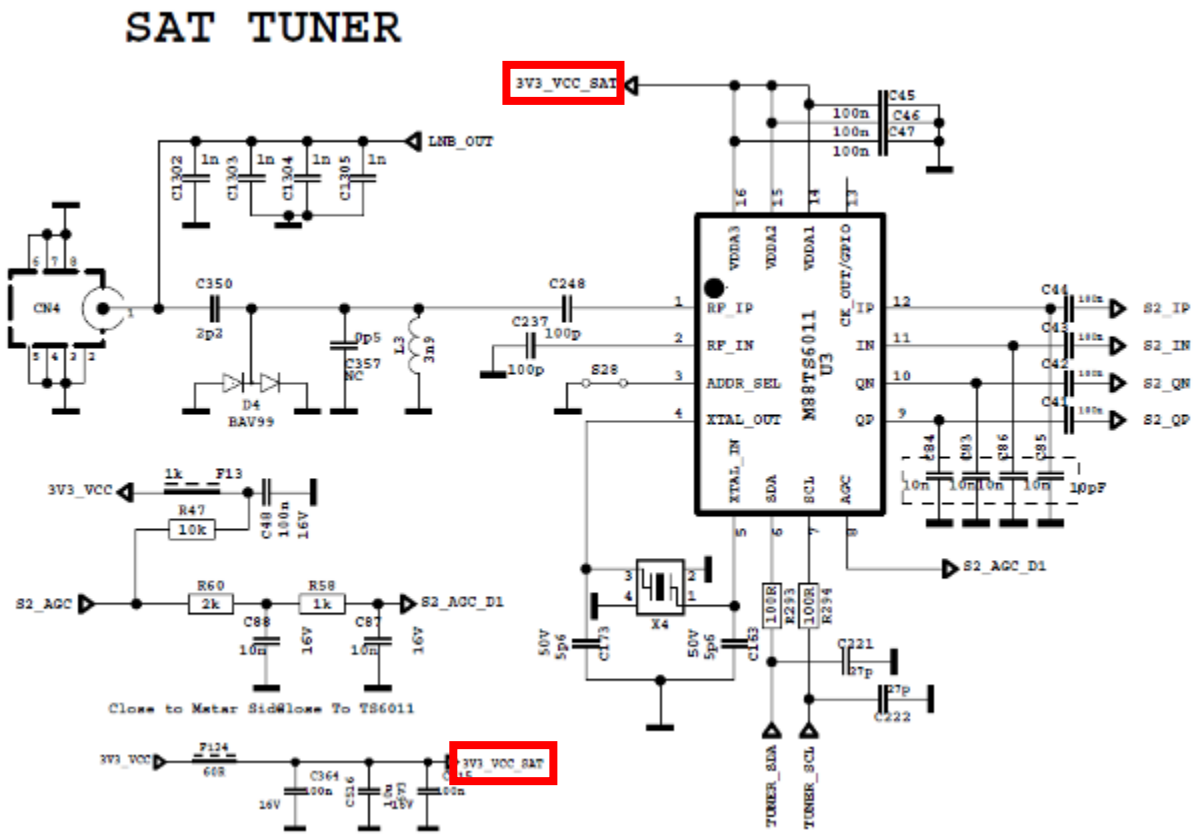
H. NO SIGNAL PROBLEM IN DVB-S/S2 MODE

Problem: No signal or Low signal in DVB-S/S2 mode.

Check signal cables and LNB voltage, if there is no problem, check M88TS6011 (U3) supply voltages; 3V3_VCC_SAT.

If the above measurements are OK, then measure the voltage from the PIN1 of U3.

If the PIN9 voltage is equal to 0V, please check i2c waveforms and software. If the PIN9 voltage is lower than 1V(e.g: 0.8Vor 0.3V), change the U3 with a new part.

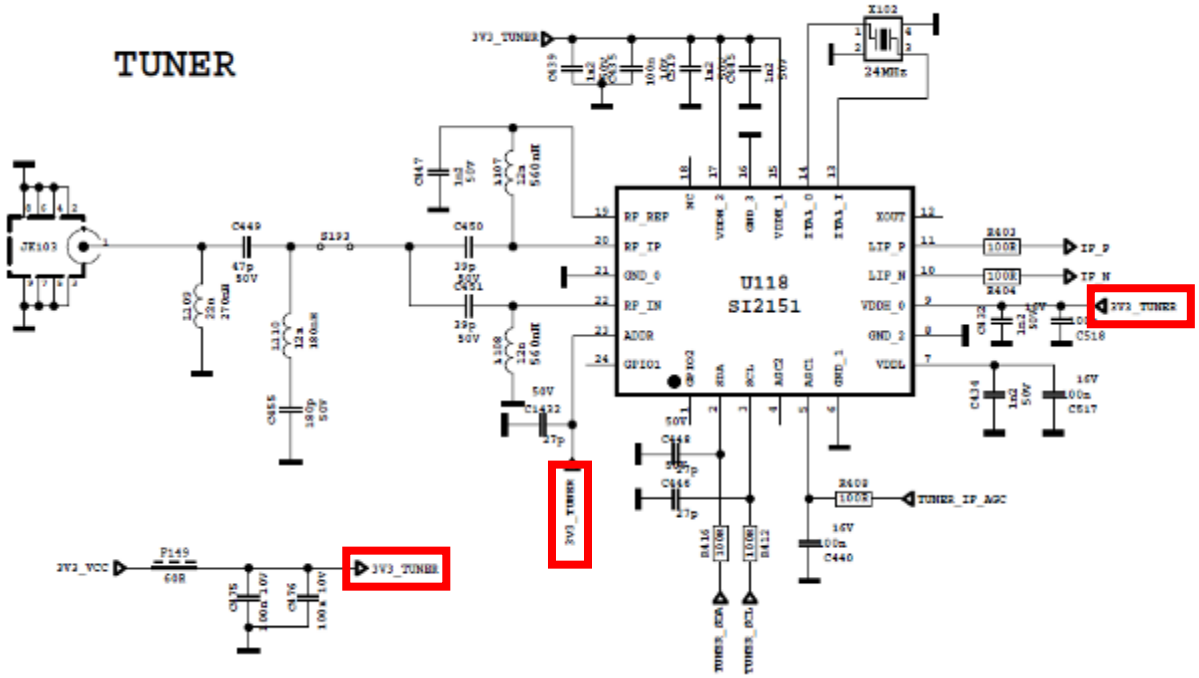


İ. NO SIGNAL PROBLEM IN DVB-T MODE

Problem: No signal or Low signal in DVB-T mode.

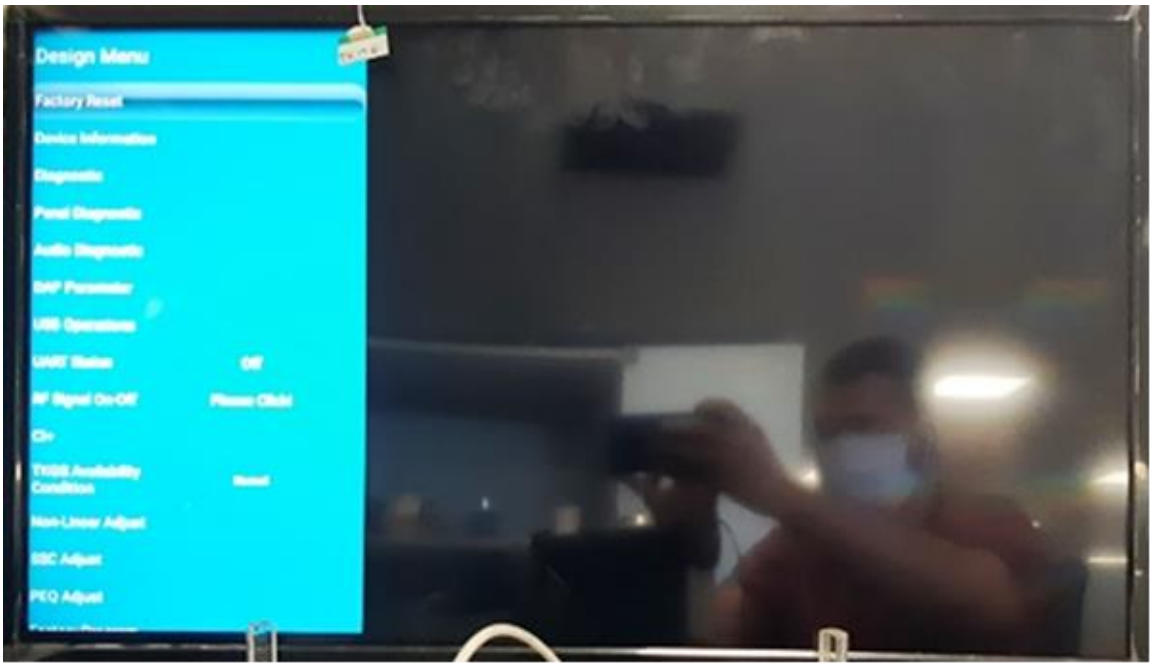
Check signal cables and LNB voltage, if there is no problem, check SI2151 (U118) supply voltages; 3V3_TUNER.

If the above measurements are OK, then change the U118 with a new part.

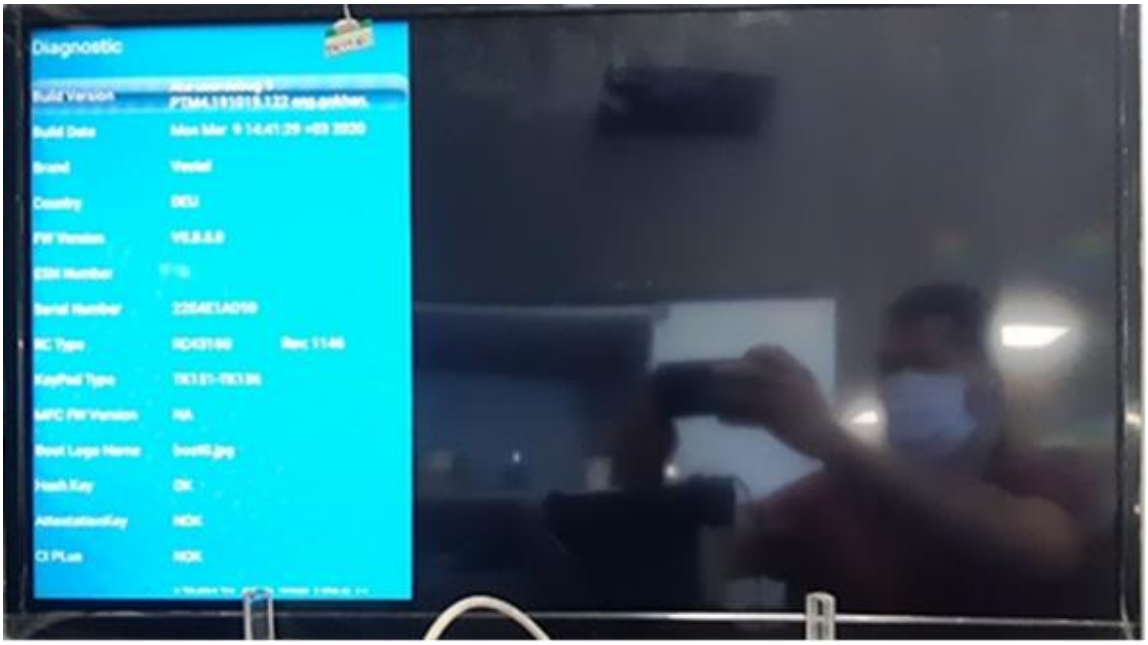


12. SERVICE MENU SETTINGS

In order to reach service menu, first chose Channel, then press **"MENU"** buton, press **"Advanced Options"** then write "**4725"** by using remote controller.
You can see the service menu main screen below. You can check SW releases by using this menu under Diagnostic title. In addition, you can make changes on video settings, audio settings, DAP Parameters etc. using regarding titles. You may also use USB Operations for SW update and update Unique Keys and Configuration files.

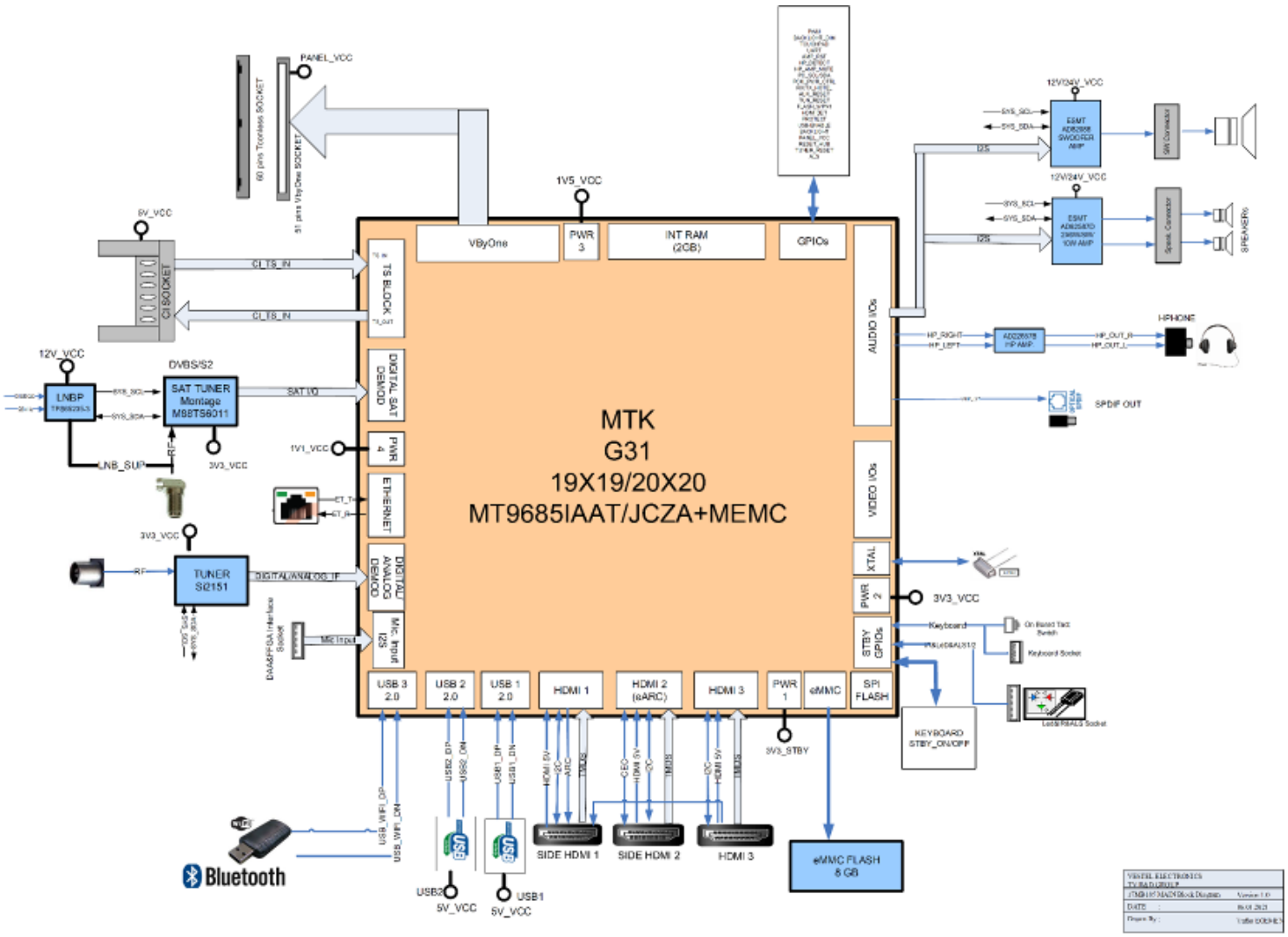


Service Menu

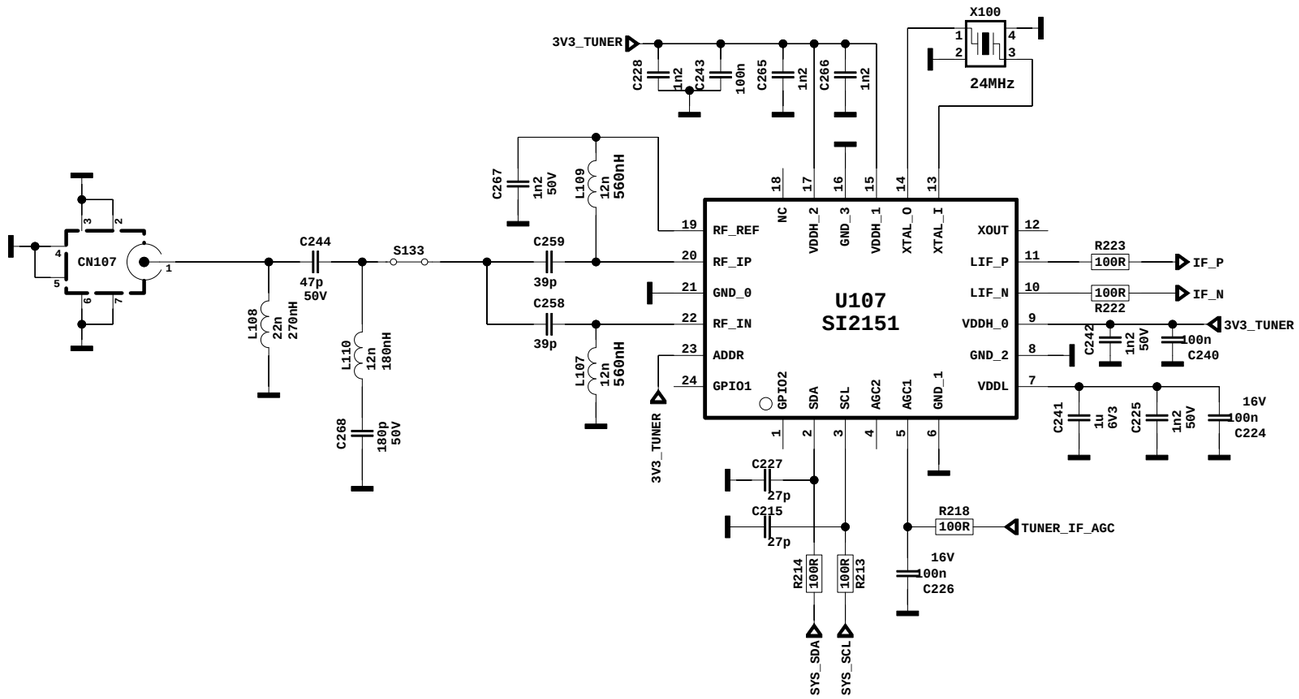


Diagnostic

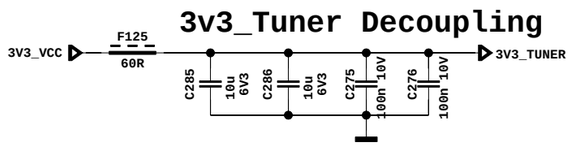
13. GENERAL BLOCK DIAGRAM



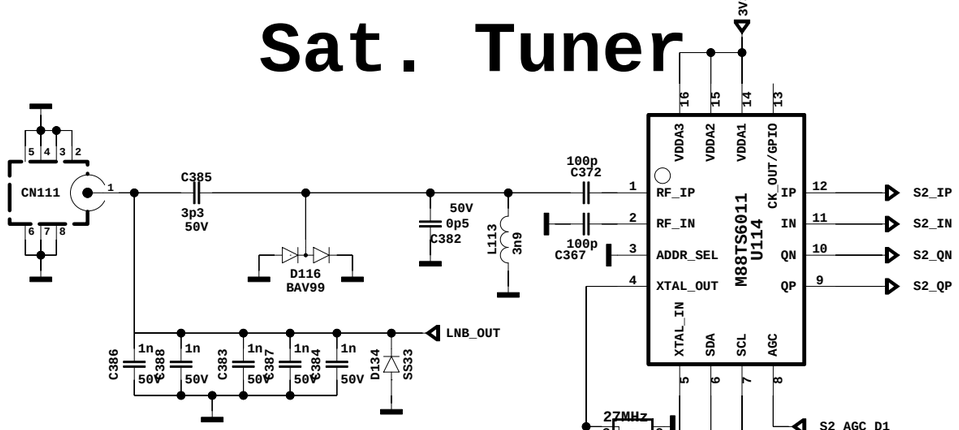
Tuner



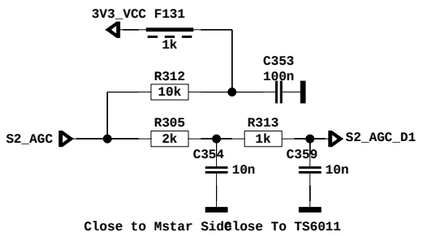
3v3_Tuner Decoupling



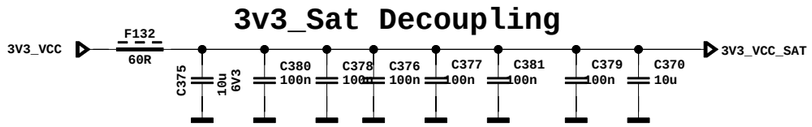
Sat. Tuner



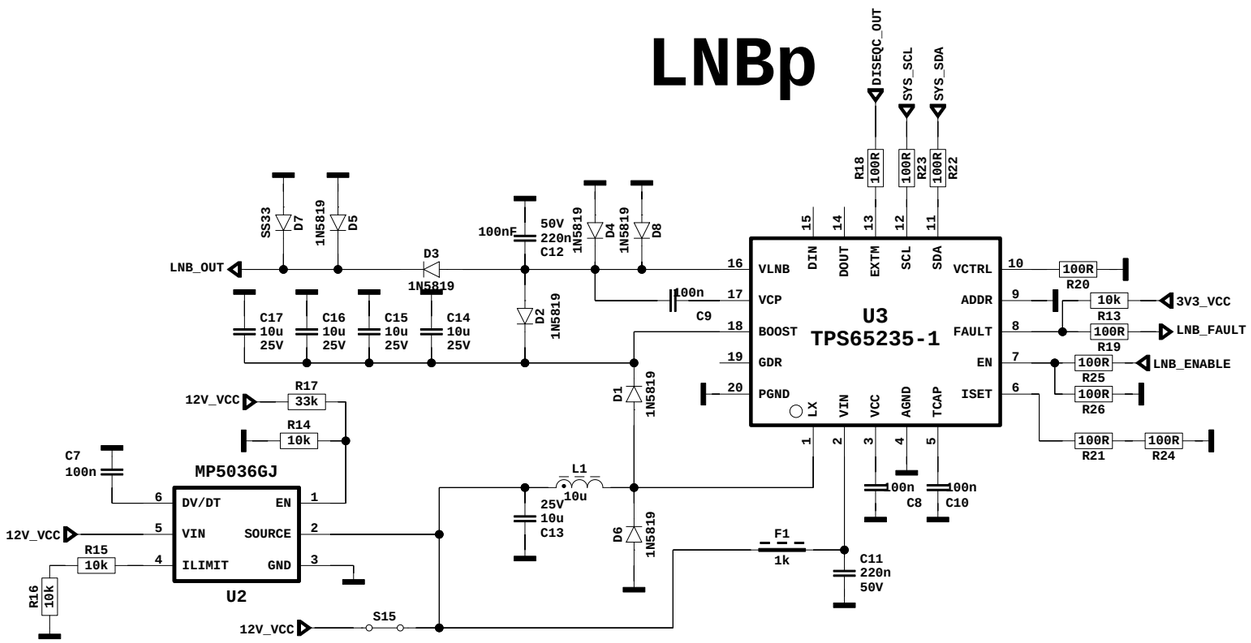
AGC Connections



3v3_Sat Decoupling



LNBp



VESTEL	PROJECT NAME : 17MB185	A3
SCH NAME :TUNER_SAT_LNB		T. SHT 8
DRAWN BY :<YOUR NAME HERE>		05/05/2021:14:44

TCONLESS/VBYONE SOCKET

CN125 CN124 CN106 CN105

CON81FE6xpVDS_51P_0.5mm_SMD_R/A_W/PL

PMIC_GPIO PAN_SDA PAN_SCL VES12N VES12P VES11N VES11P VES10N VES10P VES9N VES9P VES8N VES8P VES7N VES7P VES6N VES6P VES5N VES5P VES4N VES4P VES3N VES3P VES2N VES2P VES1N VES1P LOCKN DEMURA_CS DEMURA_DI DEMURA_DO DEMURA_CLK TCON1/GST TCON5/MCLK TCON6/GCLK TCON7/EO TCON2 TCON3 TCON0 TCON4 3V3_VCC DEMURA_WP

OP_PIN38 OP_PIN37 OP_PIN36 OP_PIN35 OP_PIN34 OP_PIN33 OP_PIN32 OP_PIN31 OP_PIN30 OP_PIN29 OP_PIN28 VBY_HTPDN VBY_LOCKN VBY_0N VBY_0P VBY_1N VBY_1P VBY_2N VBY_2P VBY_3N VBY_3P VBY_4N VBY_4P VBY_5N VBY_5P VBY_6N VBY_6P VBY_7N VBY_7P

F124 F122 F121 F120 F119

PANEL_VCC

VES12N C177 100n TP132 VBY_0N
VES12P C174 100n TP130 VBY_0P
VES11N C173 100n TP129 VBY_1N
VES11P C175 100n TP128 VBY_1P
VES10N C171 100n TP127 VBY_2N
VES10P C172 100n TP126 VBY_2P
VES9N C170 100n TP125 VBY_3N
VES9P C169 100n TP124 VBY_3P
VES8N C167 100n TP123 VBY_4N
VES8P C168 100n TP122 VBY_4P
VES7N C165 100n TP121 VBY_5N
VES7P C166 100n TP120 VBY_5P
VES6N Q161 100n TP119 VBY_6N
VES6P Q162 100n TP118 VBY_6P
VES5N C160 100n TP117 VBY_7N
VES5P C156 100n TP116 VBY_7P
VES_LOCKN F116 1k TP131 VBY_LOCKN
TCON5/MCLK F117 1k TP133 VBY_HTPDN

PANEL I2C BUFFER

PANEL_VCC R236 10k
R224 10k R230 10k
TCON_SCL BSN20 Q113 PAN_SCL
S134
PANEL_VCC R237 10k
R238 10k R239 10k
TCON_SDA Q114 BSN20 PAN_SDA
S135

S128 S126 PANEL_VCC OP_PIN38
S127 PAN_SCL PANEL_VCC R217 33k R212 10k OP_PIN37
R216 33k R211 10k OP_PIN36
S130 S215 33k R210 10k PANEL_VCC OP_PIN35
PAN_SDA S131 OP_PIN34
PAN_SCL S132 OP_PIN33
R220 33k R221 10k PANEL_VCC OP_PIN32
R207 33k R208 10k PANEL_VCC OP_PIN31
R206 33k R209 10k PANEL_VCC OP_PIN30
S123 S124 PANEL_VCC OP_PIN29
R205 33k PANEL_VCC S125 OP_PIN28

BACKLIGHT_ON/OFF_OUT AH3
GPIO0_PM_/_PWM_PM1_/_SD_CDZ_/_PM_SPI_HOLD N2
GPIO1_PM_/_PM_TX_/_PM_SPI_DO R2
GPIO5_PM_/_PM_RX_/_PM_SPI_CK AC4
GPIO6_PM_/_PM_SPI_CZ1
AMP_MUTE S1 LED2
GPIO2_PM M2
GPIO9_PM M1
GPIO10_PM Y3
MIC_PWR_CTL S163
STBY_ON/OFF P2 LED1
PWR_CTRL V5
PWM_PM H6
RESET

3V3_STBY R248 1k C299 100n 10V C298 100n 16V D108 1N4148 R247 10k C295 100n 10V

DDCR_CK B20
DDCR_DA A20
DDCA_CK J4
DDCA_DA J5
SAR0 AC5
SAR1 Y8
SAR2 AC9
SAR3 AB9
VPLUGIN H5
VID0 U5
VID1 P7
VID2 P3
LD_SPI_MISO_/_SPI2_DI E14
LD_SPI_CS_/_SPI2_CK D17
LD_SPI_MOSI_/_SPI1_DI E17
LD_SPI_CK_/_SPI1_CK D14
GPIO0 E18

3V3_STBY R244 4k7 TP191 DEBUG_RX DEBUG_TX
3V3_STBY R241 4k7 TP192
KEYBOARD
3V3_STBY R382 4k7 D123 PESD9M5VH
PANEL_VCC_ON/OFF R10
WOWL_DET
POWER_SENSE
CORE_VID0 CPU_VID1 CPU_VID2
DEMURA_DO DEMURA_DI DEMURA_CLK 4k7 R385 R387 R388 C157 50V 10p DEMURA_CS

U108

MT9685LAAJAC

LVSYNC_/_Mini_A_5-_/_VX1_0- C1 VES12N
LHSYNC_/_Mini_A_5+_/_VX1_0+ C2 VES12P
LDE_/_Mini_A_4-_/_VX1_1- B1 VES11N
LCK_/_Mini_A_4+_/_VX1_1+ B2 VES11P
LVB0-_/_Mini_A_3-_/_VX1_2- B3 VES10N
LVB0+_/_Mini_A_3+_/_VX1_2+ A3 VES10P
LVB1-_/_Mini_A_CK-_/_VX1_3- C3 VES9N
LVB1+_/_Mini_A_CK+_/_VX1_3+ B4 VES9P
LVB2-_/_Mini_A_2-_/_VX1_4- C4 VES8N
LVB2+_/_Mini_A_2+_/_VX1_4+ B5 VES8P
LVBCLK-_/_Mini_A_1-_/_VX1_5- A5 VES7N
LVBCLK+_/_Mini_A_1+_/_VX1_5+ C5 VES7P
LVB3-_/_Mini_A_0-_/_VX1_6- A6 VES6N
LVB3+_/_Mini_A_0+_/_VX1_6+ B6 VES6P
LVB4-_/_Mini_B_5-_/_VX1_7- C6 VES5N
LVB4+_/_Mini_B_5+_/_VX1_7+ B7 VES5P
LVA0-_/_Mini_B_4-_/_Vx1_OSD_00- B8 VES4N
LVA0+_/_Mini_B_4+_/_Vx1_OSD_00+ C8 VES4P
LVA1-_/_Mini_B_3-Vx1_OSD_01- B9 VES3N
LVA1+_/_Mini_B_3+_/_Vx1_OSD_01+ A9 VES3P
LVA2-_/_Mini_B_CK-_/_Vx1_OSD_02- C9 VES2N
LVA2+_/_Mini_B_CK+_/_Vx1_OSD_02+ A10 VES2P
LVACLK-_/_Mini_B_2-_/_Vx1_OSD_03- B10 VES1N
LVACLK+_/_Mini_B_2+_/_Vx1_OSD_03+ C10 VES1P
LVA3-_/_Mini_B_1-_/_LOCKN B11 VES_LOCKN
LVA3+_/_Mini_B_1+_/_HTPDN C11 TCON5/MCLK
LVA4-_/_Mini_B_0-_/_OSD_LOCKn B12 10k 3V3_VCC
LVA4+_/_Mini_B_0+_/_OSD_HTPDn C12 R183 10k 3V3_VCC R185
S117 TCON6/GCLK
S118 TCON7/EO

Mini_C_5- F4
Mini_C_5+ F3
Mini_C_4- F5
Mini_C_4+ F6
Mini_C_3- E2
Mini_C_3+ E3
Mini_C_CK- D2
Mini_C_CK+ D1
Mini_C_2- E5
Mini_C_2+ E4
Mini_C_1- D4
Mini_C_1+ D5
Mini_C_0- D6
Mini_C_0+ D7
Mini_D_5- E7
Mini_D_5+ F7
Mini_D_4- E8
Mini_D_4+ E9
Mini_D_3- D8
Mini_D_3+ D9
Mini_D_CK- D10
Mini_D_CK+ E10
Mini_D_2- F11
Mini_D_2+ E11
Mini_D_1- D11
Mini_D_1+ D12
Mini_D_0- E12
Mini_D_0+ F12

R6 4k7 R7 4k7 R8 4k7 R5 4k7 R9

TCON0 C13 S115 TCON0
TCON1 A14 S116 TCON1/GS
TCON2 B14 S113 TCON2
TCON3 C14 S110 TCON3
TCON4 B15 S114 TCON4

GPIO11 M3 AMP_RST
GPIO12 L3 HP_DETECT
R393 10k 3V3_VCC

PWM0 A19 BACKLIGHT_DIM
PWM1 C17
PWM2 C19 FF_LED

TESTPIN D18

R1 3V3_STBY 4k7
BT_WAKE U2 GPIO7_PM
USB_ENABLE_1 AB4 GPIO8_PM
WOWL_EN H1 GPIO11_PM
WIFI_RST M4 GPIO12_PM
3V3_STBY R432 4k7

LNB_FAULT AD16 GPIO9
LNB_ENABLE AC16 GPIO10

1V8 TCON Level Shifter

S119 Q112 VES_LOCKN LOCKN
PANEL_VCC R181 10k R187 10k R182 10k

CHIP CONFIGURATION

CHIP_CONFIG[2:0]={PAD_PM_GPIO9,PAD_PM_GPIO10,PAD_PM_GPIO2}

3V3_STBY R246 4k7 nc GPIO9_PM GPIO9_PM R245 4k7
3V3_STBY R260 4k7 GPIO10_PM GPIO10_PM R256 4k7 nc
3V3_STBY R272 4k7 nc GPIO2_PM GPIO2_PM R271 4k7

CN101 75LG_VCC
6 PANEL_VCC
1 C103 100n 10V C104 100n 10V
2
3
4
5
7

F101 12V_STBY F103 FDC642P Q101 C110 220n 25V 33k R106 R111 47R
FS102 7A/32VDC S209 TP103 PANEL_VCC
Q100 FDS4685 12V_STBY R107 47R fds4685
R164 33k R153 4k7 3V3_STBY R152 10k PANEL_VCC_ON/OFF Q109 BC848B C141 1n 50V

* JUST ONE OF THEM SHOULD BE USED

opt.

12V_VCC R273 10k R274 1k POWER_SENSE
needs GND shielding
R275 1k D109 C3V6 C325 330p

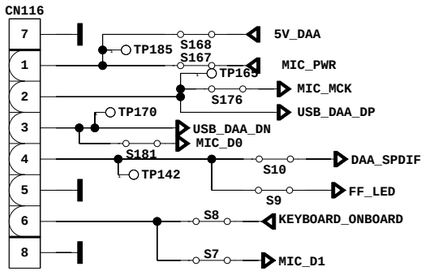
UART DEBUG

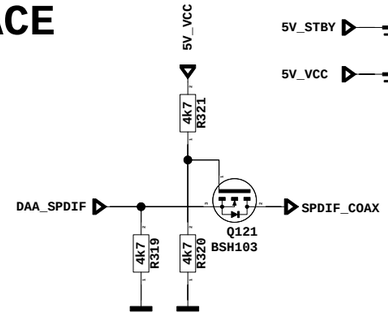
DEBUG_TX DEBUG_RX S137 S136 CN108 5 1 2 3 4 6

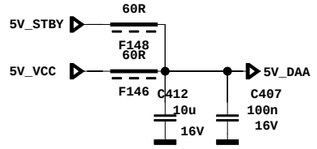
Value	Description
3'b010	ARM boot from ROM; outer storage is eMMC
3'b011	ARM boot from ROM; outer storage is NAND

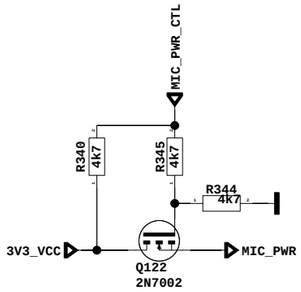
VESTEL	PROJECT NAME : 17MB185	A3
	SCH NAME :VBYONE	T. SHT 8
	DRAWN BY :<YOUR NAME HERE>	30/04/2021:15:43

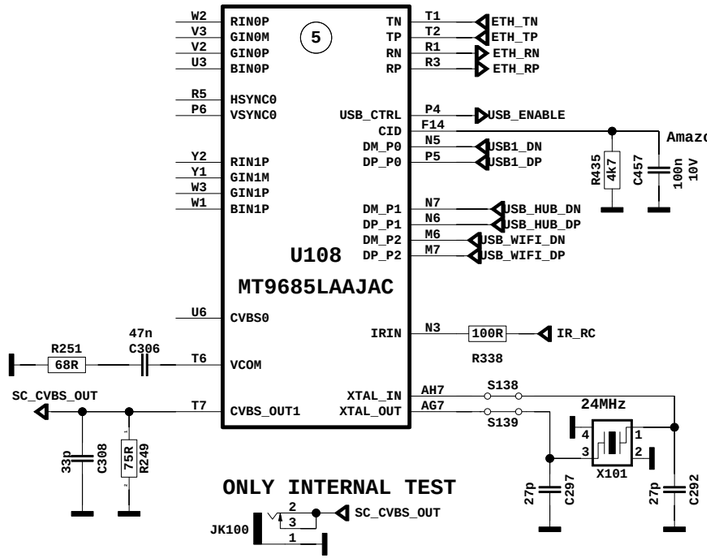
DAA/FFGA INTERFACE

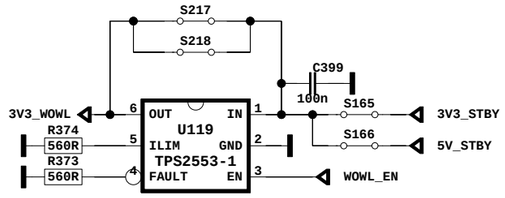




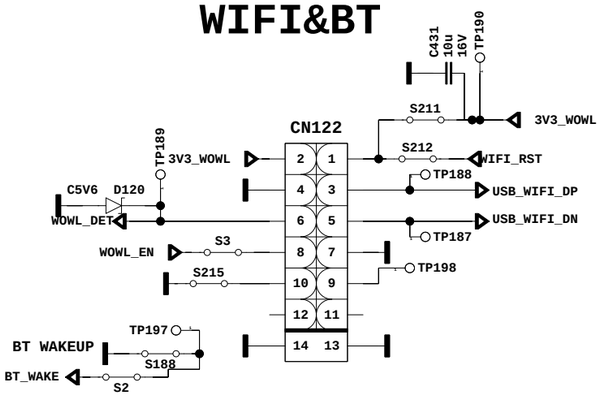




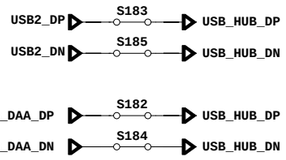




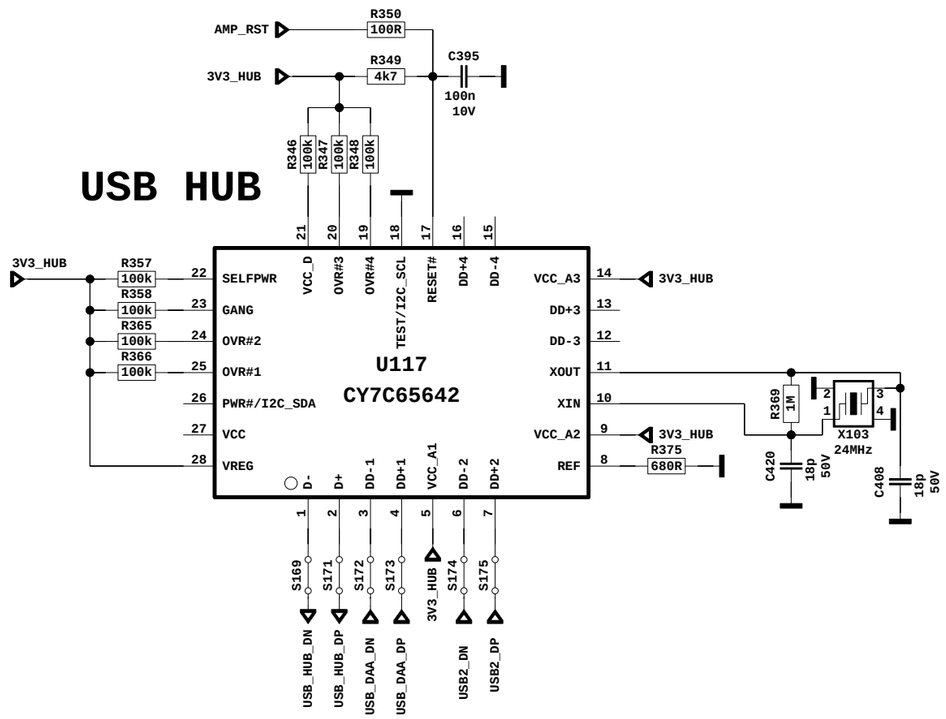
WIFI&BT



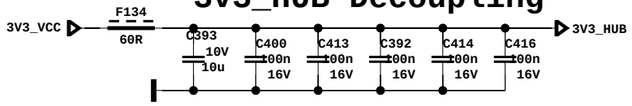
HUB BYPASS

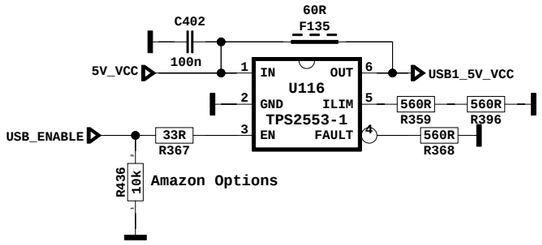


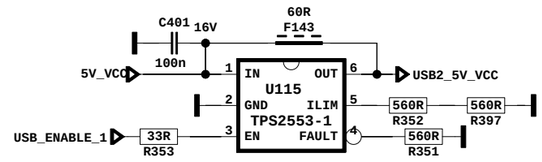
USB HUB



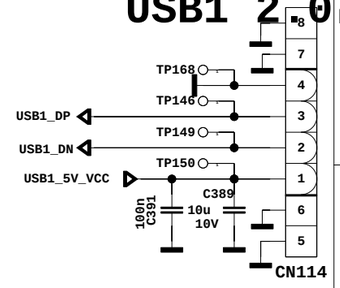
3v3_HUB Decoupling



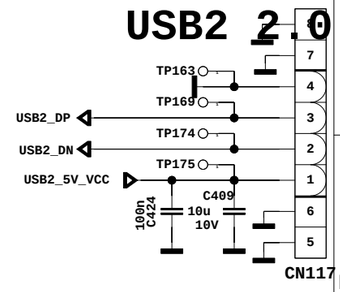




USB1 2.0



USB2 2.0



VESTEL	PROJECT NAME : 17MB185	A3
SCH NAME :USB		T. SHT 8
DRAWN BY :<YOUR NAME HERE>		14/07/2021:17:44

HDMI1 (SIDE)

CN109

HDMI0_RX2P
HDMI0_RX2N
HDMI0_RX1P
HDMI0_RX1N
HDMI0_RX0P
HDMI0_RX0N
HDMI0_CLKP
HDMI0_CLKN
CEC
HDMI0_SCL
HDMI0_SDA
HDMI0_5V

R277 470R DEBUG_RX
R257 33R
R261 33R
R258 47k
R259 47k
TP2 TP3 TP4 TP6 TP5
R283 470R DEBUG_TX
C328 15p 50V
R457 1k
R456 1k
R441 10k
R440 10k
Q130 BC848B
Q129 BC848B
5V_VCC
R263 33R HOTPLUG0

HDMI0_5V R262 33R R453 33R
HDMI2_5V R315 33R R454 33R HOTPLUG0

HDMI0_RX0N AF14
HDMI0_RX0P AG14
HDMI0_RX1N AF15
HDMI0_RX1P AG15
HDMI0_RX2N AF16
HDMI0_RX2P AG16
HDMI0_CLKN AH13
HDMI0_CLKP AG13
HDMI0_SCL AD11
HDMI0_SDA AD12
HOTPLUG0 AE11
AC12
HDMI2_RX0N AG10
HDMI2_RX0P AF11
HDMI2_RX1N AG11
HDMI2_RX1P AF12
HDMI2_RX2N AG12
HDMI2_RX2P AH12
HDMI2_CLKN AG9
HDMI2_CLKP AF10
HDMI2_SCL AC13
HDMI2_SDA AD13
HOTPLUG2 AB13
AB12
HDMI1_RX0N AB2
HDMI1_RX0P AB3
HDMI1_RX1N AC2
HDMI1_RX1P AC3
HDMI1_RX2N AD2
HDMI1_RX2P AD3
HDMI1_CLKN AA3
HDMI1_CLKP AB1
HDMI1_SCL W7
HDMI1_SDA V7
HOTPLUG1 V6
U4

HDMI1_5V R332 33R R455 33R

AF1
AF2
AG1
AG2
AG3
AH2
AE1
AE3
W5
W6
Y4
Y7

CEC R308 100R AD14
HDMI_ARCN C442 6V3 1u AE15
HDMI_ARCP C347 6V3 1u S151 AD15

3

U108
MT9685LAAJAC

A_RX0N
A_RX0P
A_RX1N
A_RX1P
A_RX2N
A_RX2P
A_RXCN
A_RXCP
DDCDA_CK
DDCDA_DA
HOTPLUGA
HOTPLUGA_HDMI20_5V
B_RX0N
B_RX0P
B_RX1N
B_RX1P
B_RX2N
B_RX2P
B_RXCN
B_RXCP
DDCDB_CK
DDCDB_DA
HOTPLUGB
HOTPLUGB_HDMI20_5V
C_RX0N
C_RX0P
C_RX1N
C_RX1P
C_RX2N
C_RX2P
C_RXCN
C_RXCP
DDCDC_CK
DDCDC_DA
HOTPLUGC
HOTPLUGC_HDMI20_5V
D_RX0N
D_RX0P
D_RX1N
D_RX1P
D_RX2N
D_RX2P
D_RXCN
D_RXCP
DDCDD_CK
DDCDD_DA
HOTPLUGD
HOTPLUGD_HDMI20_5V
CEC0
NC
HDMIRX_ARCTXP

LINEIN_L0 AE5
LINEIN_R0 AF5
LINEOUT_L0 AE6
LINEOUT_R0 AF6
EARPHONE_OUTL AF4
EARPHONE_OUTR AH4
VAG AG5
VRM_ADC AH5
I2S_OUT_MCK K2
I2S_OUT_BCK H2
I2S_OUT_WCK K3
I2S_OUT_SD0 J2
I2S_OUT_SD1 J3
I2S_OUT_SD2 K4
SPDIF_IN L1
SPDIF_OUT L2
I2S_IN_BCK K6
I2S_IN_WCK K5
I2S_IN_DIN0 K7
I2S_IN_DIN1 L4
I2S_IN_DIN2 L5
DMIC_BCK B17
DMIC_SD0 C18
DMIC_SD1 B18
DMIC_SD2 B19
MICIN1 AA5
MICCM1 AA6
MICIN0 AB5
MICCM0 AB6

3n3 C323
3n3 C322
S144
S143
C396 100n 16V
HP_LEFT
HP_RIGHT
CLOSE TO MSTAR IC
C296 100n 16V
220R F126
TCON_SCL
TCON_SDA
4k7 R250
3V3_VCC
4k7 R12
CI_PWR_CTL
S179 MIC_MCK
S180 MIC_D0
S11 MIC_D1

HOTEL TV OPTIONS

ETH_PIN1 S159 R282 10k 3V3_STBY
S146 DEBUG_RX
ETH_PIN2 S156 R281 10k 3V3_STBY
S148 DEBUG_TX

R1 R2 R3 R4 22R
AOLRCK
AOSDATA0
AOMCLK
AOBCK
12p C319
12p C321
R255 R4 R3 R2 R1 22R
AOLRCK_SW
AOSDATA0_SW
AOBCK_SW
C318 12p

ETHERNET

CN112

ETH_TP S158 ETH_PIN1 TD+
ETH_TN S157 ETH_PIN2 TD-
TCT
TP158 5V_STBY F139 1k C397 1u
RD+ ETH_RP S155
RD- ETH_RN S154
TP156 5V_STBY F141 1k C404 1u
RCT
NC1 IR_FROM_ETH S164
NC2
SHLD1
SHLD2

IR_FROM_ETH Q123 BC848B IR_RC
R354 10k 5V_STBY

LED&IR&ALS

5V_VCC F154 1k C429 100n
3V3_VCC F147 1k
ALS_SCL
ALS_SDA
SYS_SCL S13 ALS_SCL
SYS_SDA S12 ALS_SDA

CN120 2 4 6 8 10 / 1 3 5 7 9
TP179 TP164 TP159 TP161 TP108
CN119 1 2 3 4 5 6
CN118 1 2 3 4 5
KEYBOARD_ONBOARD

5V_STBY D119 C5V6 IR_RC
F140 1k
R378 150R
C403 27p 50V

LED2 R361 10k
Q126 BC848B
10k R376
220R R360
220R R370
10k R379
Q127 BC848B
10k R362 LED1
Q125 BC858B
Q128 BC858B
10k R446
10k R447
220R R377
220R R380
5V_STBY

TACT SWITCH

TP101
R102 47R KEYBOARD_ONBOARD
R101 4k7
C108 100n 10V
D100 BZT52C5V6LP
SW100

HDMI2 (SIDE ARC)

CN110

HDMI2_RX2P
HDMI2_RX2N
HDMI2_RX1P
HDMI2_RX1N
HDMI2_RX0P
HDMI2_RX0N
HDMI2_CLKP
HDMI2_CLKN
CEC
HDMI_ARCP
HDMI2_SCL
HDMI2_SDA
HDMI2_5V

S153 TP14 TP13 TP12 TP8
R309 33R
R314 33R
R310 47k
R311 47k
R434 47k
R4k7 4k7
R316 33R HOTPLUG2
R452 33R HDMI_ARCN

HDMI2_5V
R459 1k
5V_VCC
R458 1k
Q132 BC848B
R443 10k
Q131 BC848B
R442 10k HOTPLUG2

KEYBOARD

KEYBOARD_ONBOARD
R342 10k 3V3_STBY
R341 47R
1k F133
F138 1k
PESD9N5VH D132
KEYBOARD TP152
3V3_STBY

CN115 1 2 3 4 5 6
TP153 TP155 TP157 TP160 TP162
D117 CDA4C166TH 4 3 2 1 / 5 6 7 8

DIMMING

TP110 BACKLIGHT_DIM
S106
BSH103 Q105
DIMMING
R143 10k
R142 10k
5V_VCC
R141 4k7

e-ARC

HOTPLUG2
200R R410 10k
22n L118 60R F152
HDMI_ARCN
5.1K R415 47k

HDMI2_5V
R411 10k 1.2K
22n L119 60R F153
HDMI_ARCP
R412 10k
R416 47k 5.1K

HDMI3 (BACK)

CN113

HDMI1_RX2P
HDMI1_RX2N
HDMI1_RX1P
HDMI1_RX1N
HDMI1_RX0P
HDMI1_RX0N
HDMI1_CLKP
HDMI1_CLKN
CEC
HDMI1_SCL
HDMI1_SDA
HDMI1_5V

TP7 TP10 TP11 TP9
R335 33R
R334 33R
R336 47k
R337 47k
R333 33R HOTPLUG1

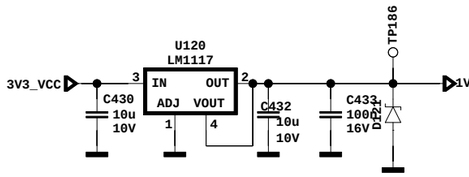
HDMI1_5V
R461 1k
5V_VCC
R460 1k
Q134 BC848B
R445 10k
Q133 BC848B
R444 10k HOTPLUG1

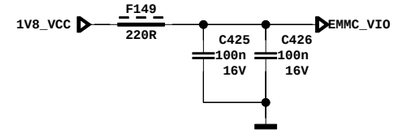
SPDIF OUT

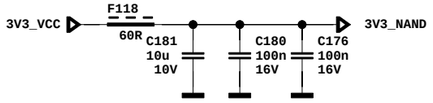
FB100
VIN 1
VCC 2
GND 3
SPDIF_COAX
F130 1k 5V_VCC
R318 4k7 10V
100n C351
Q120 BC848B
C357 100n 10V
R324 100R SPDIF_OUT
R317 4k7
C356 22p 50V
TP148 SPDIF_COAX
JK101 2 3 1
TP145
C363 100n 10V
220R R325
C364 22p 50V
R326 220R

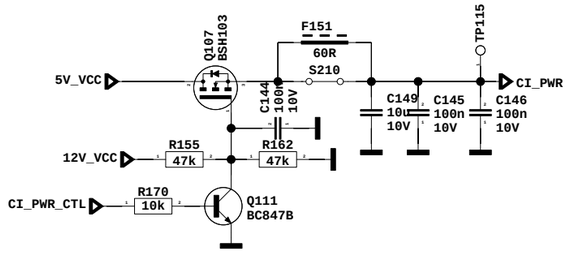
VESTEL	PROJECT NAME : 17MB185	A3
SCH NAME :HDMI_GPIO		T. SHT8
DRAWN BY :<YOUR NAME HERE>		10/05/2021:14:09

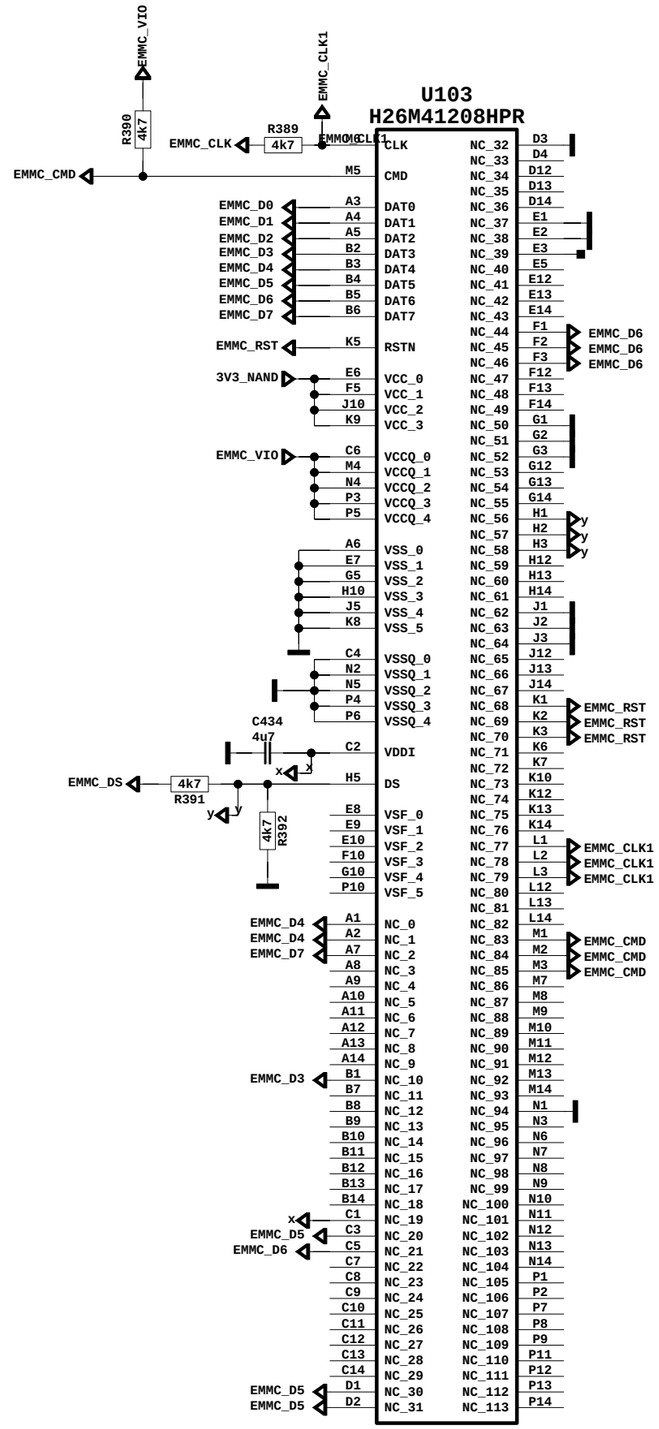
1V8_VCC LDO



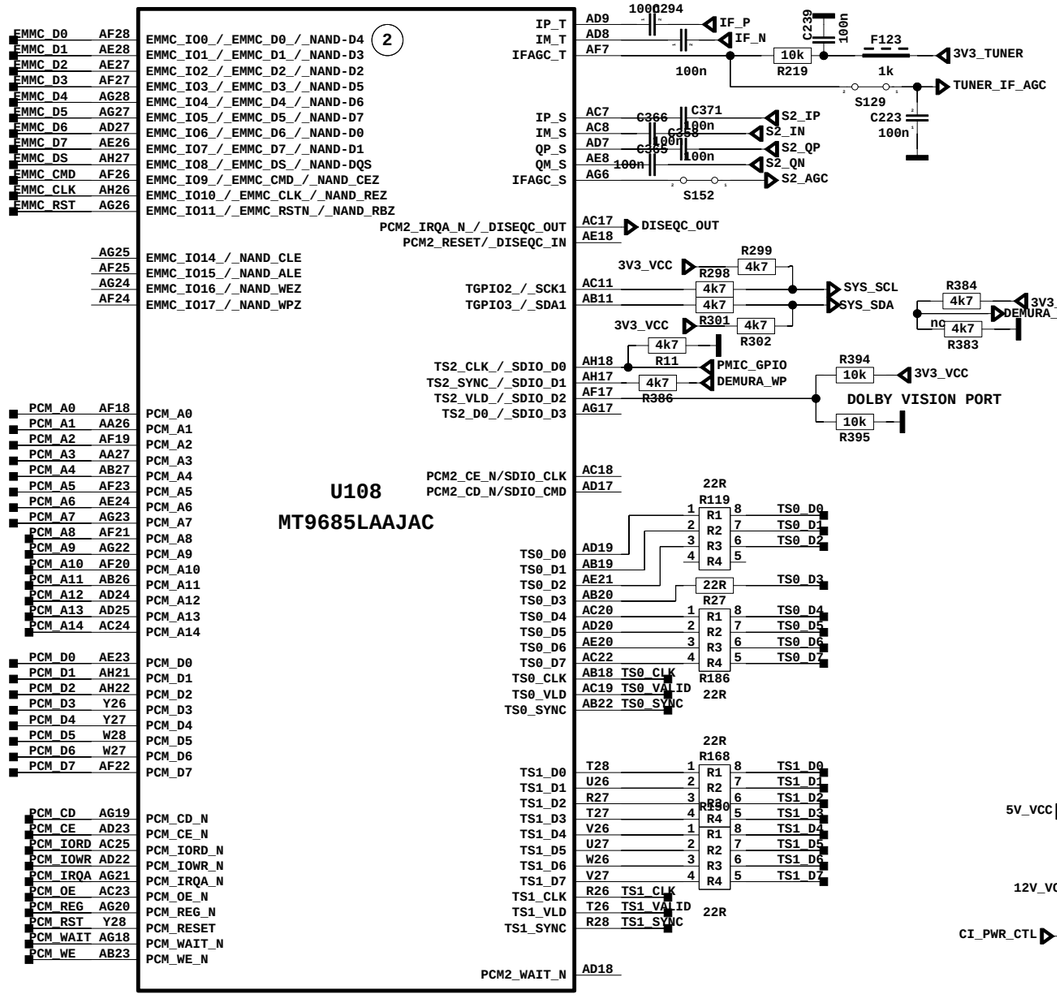




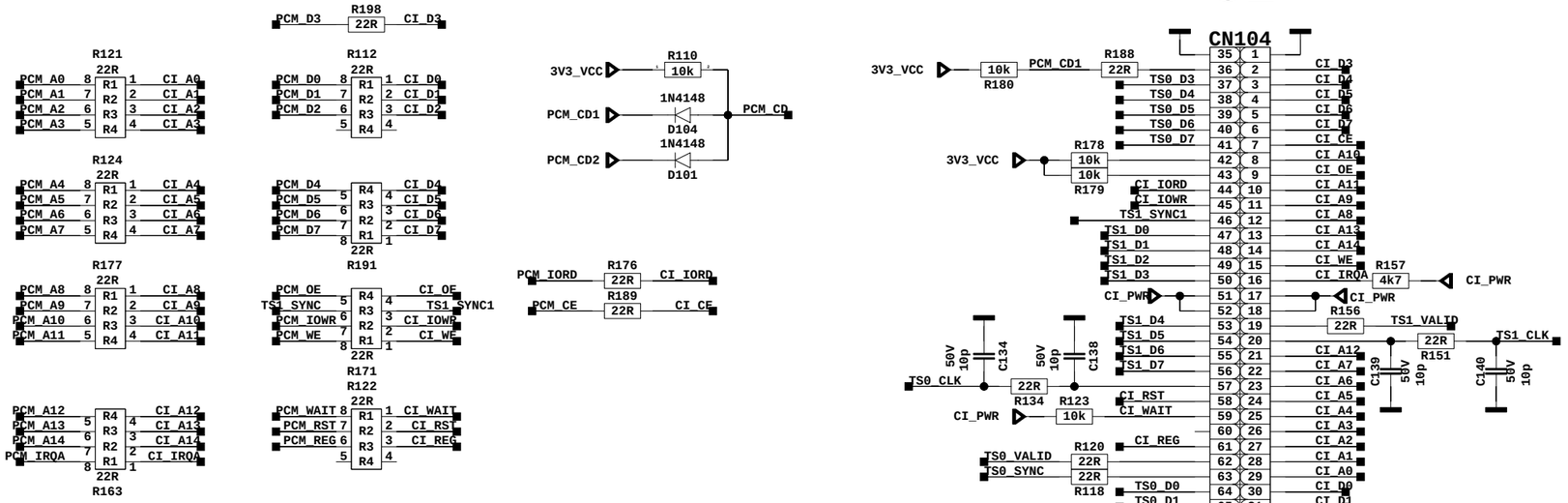




U108
MT9685LAAJAC

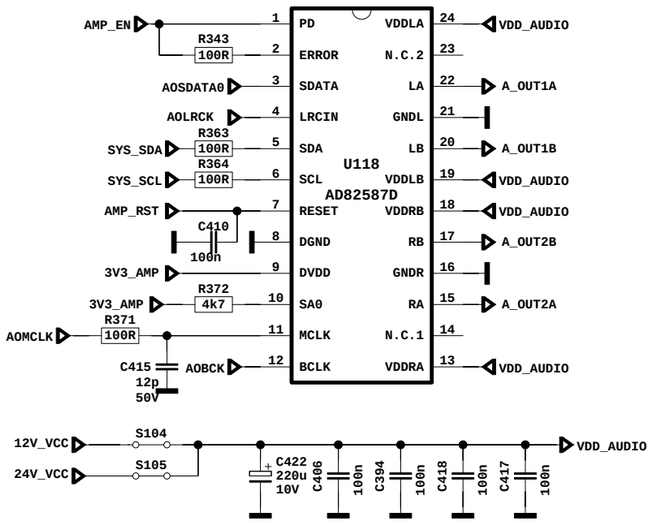


CI

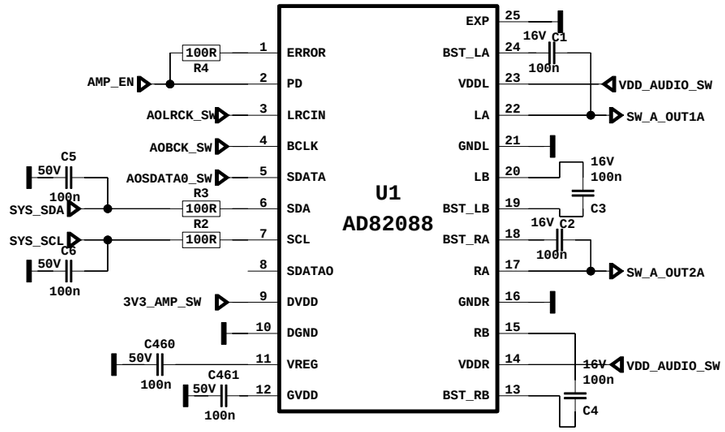


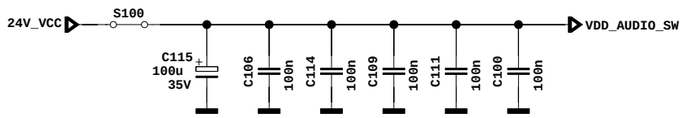
VESTEL	PROJECT NAME : 17MB185	A3
SCH NAME :CI_EMMC		T. SHT 8
DRAWN BY :<YOUR NAME HERE>		04/05/2021:12:30

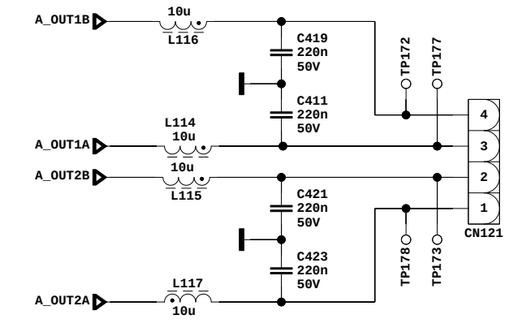
MAIN AMP
6W/8W/10W

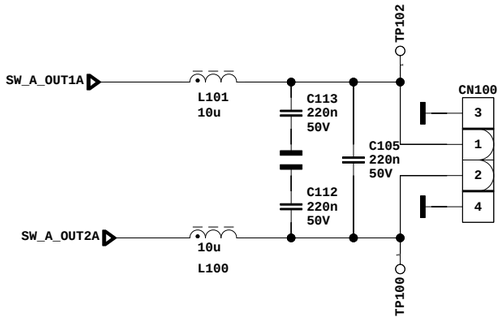


SUBWOOFER AMP

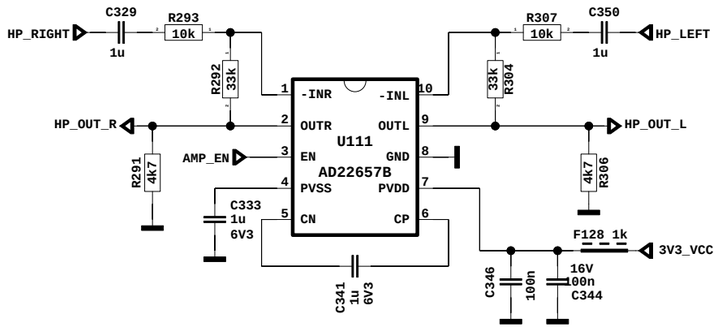




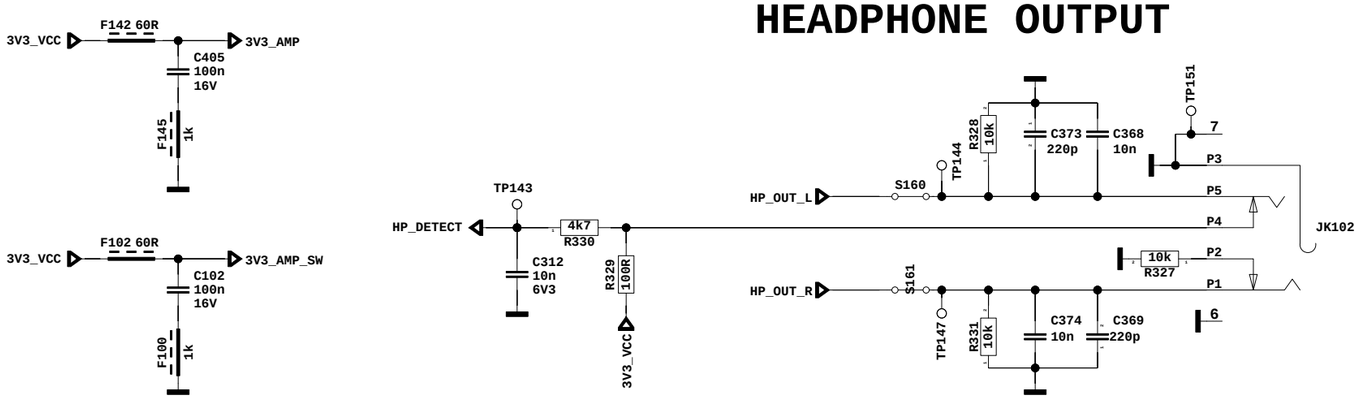




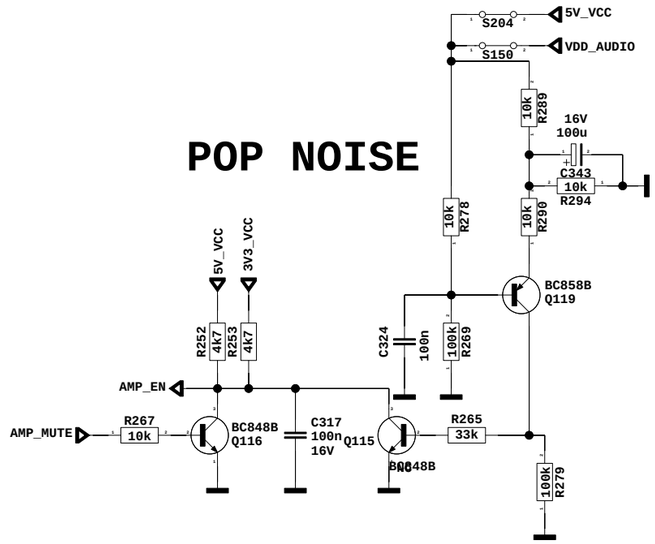
HEADPHONE AMP



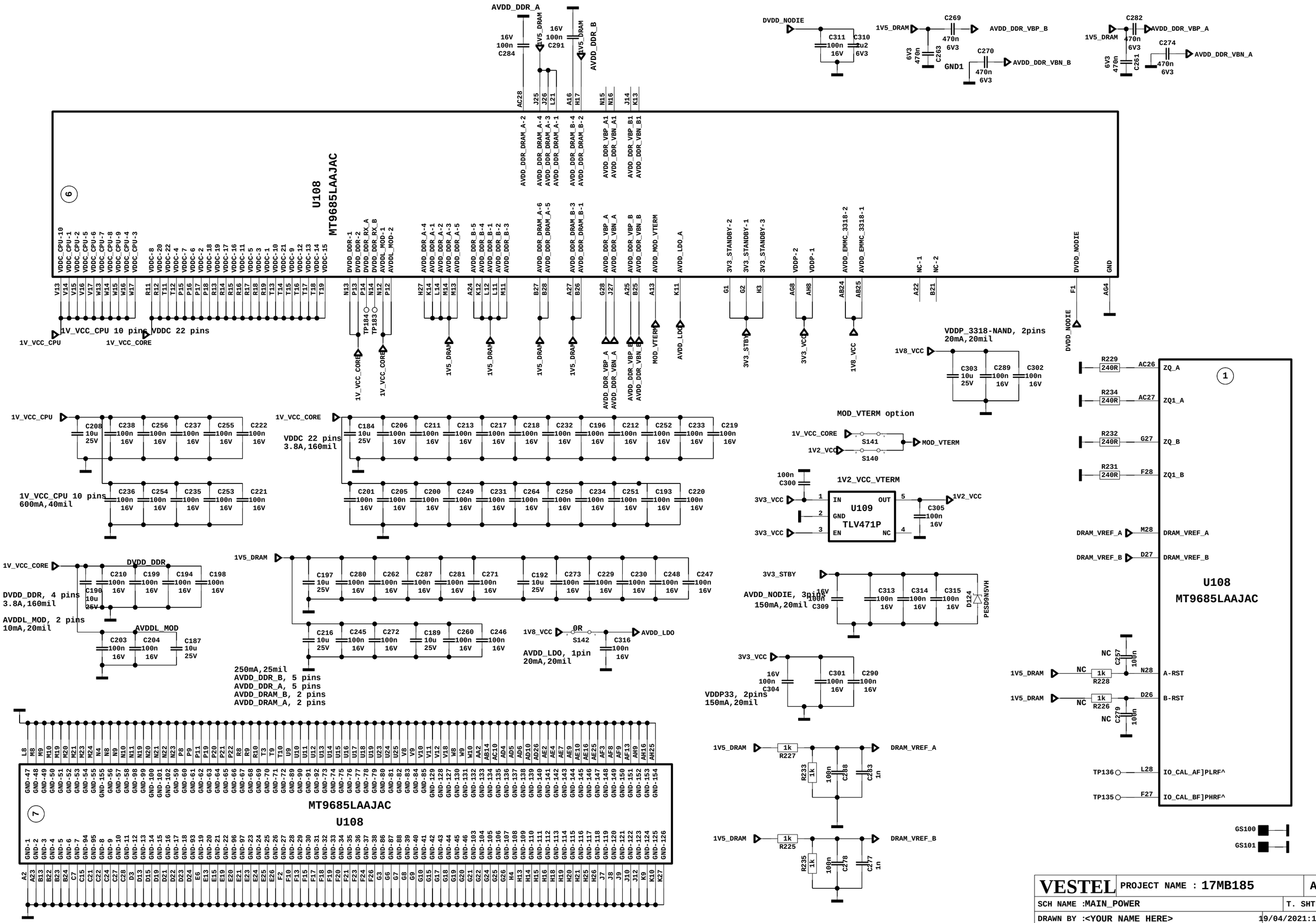
HEADPHONE OUTPUT



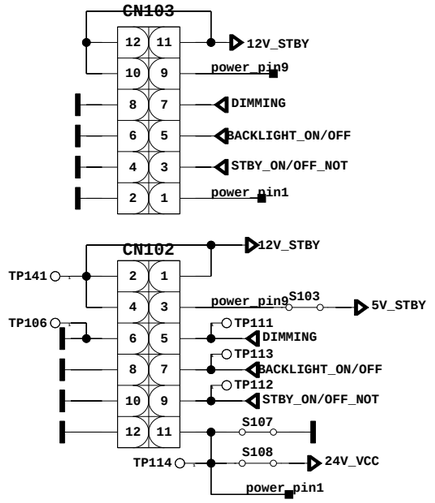
POP NOISE



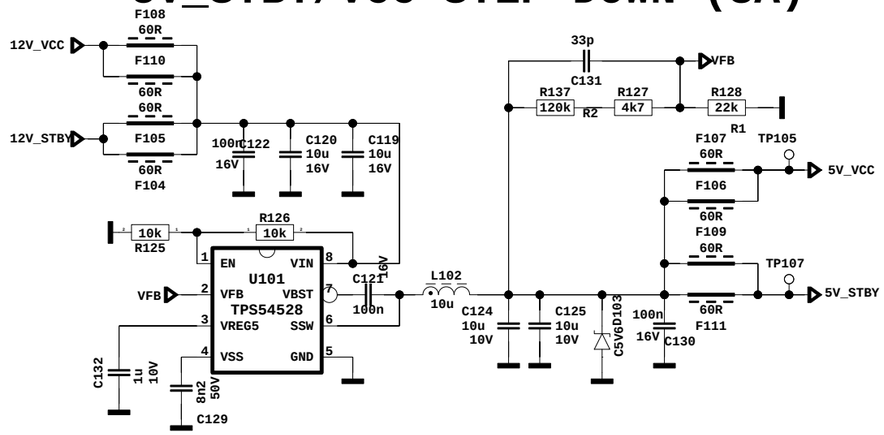
VESTEL	PROJECT NAME : 17MB185	A3
SCH NAME :AUDIO AMPs		T. SHT 8
DRAWN BY :<YOUR NAME HERE>		10/05/2021:14:01



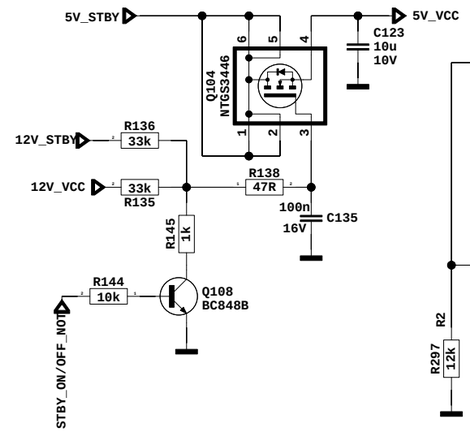
VESTEL	PROJECT NAME : 17MB185	A3
SCH NAME :MAIN_POWER		T. SHT 8
DRAWN BY :<YOUR NAME HERE>		19/04/2021:11:16



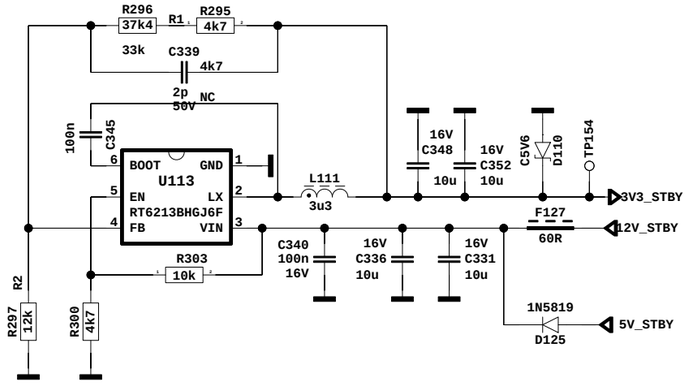
5V_STBY/VCC STEP-DOWN (3A)



5V_VCC SWITCH

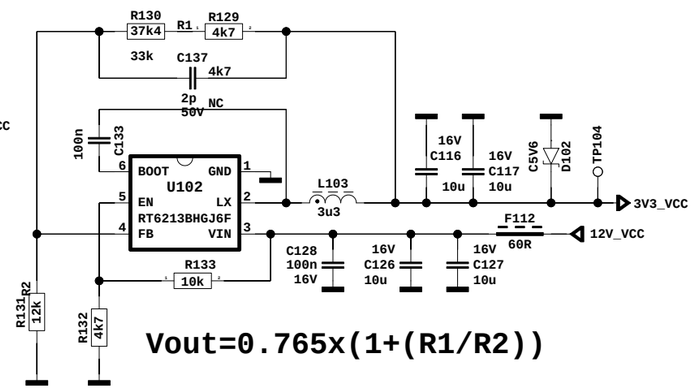


3V3_STBY DC/DC (2A)



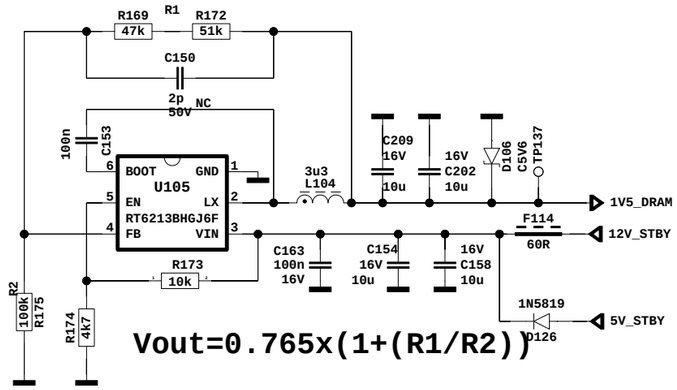
12V_VCC SWITCH

3V3_VCC DC/DC (3A)



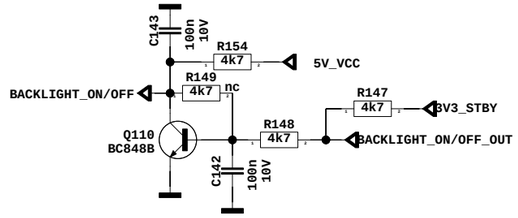
Vout=0.765x(1+(R1/R2))

1V5_DRAM DC/DC (2A)

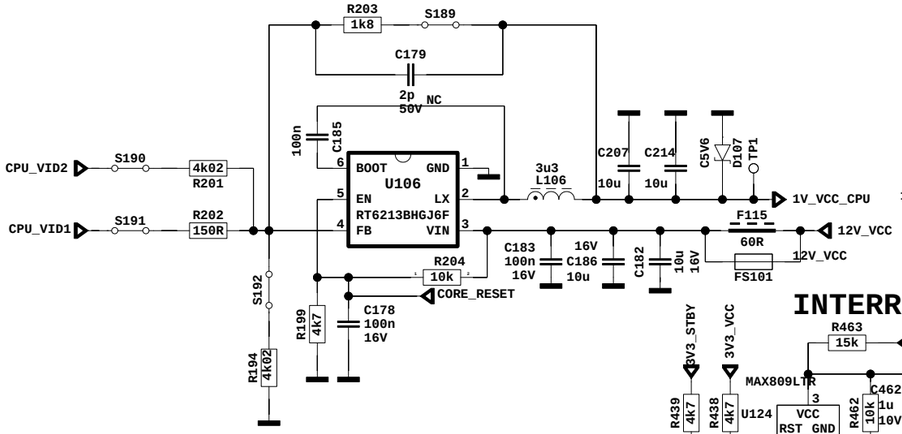


Vout=0.765x(1+(R1/R2))

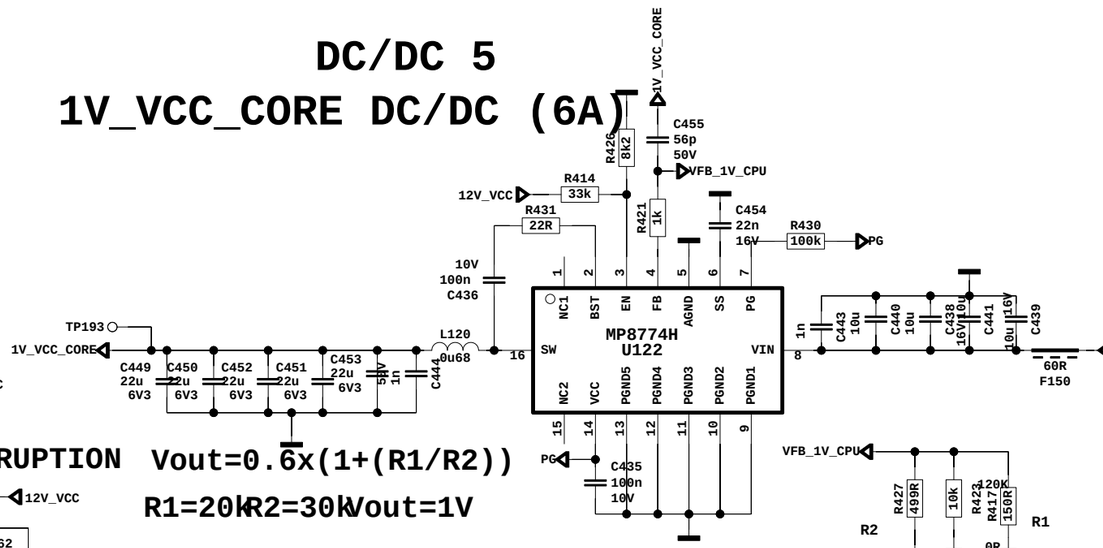
Backlight On/Off Circuit



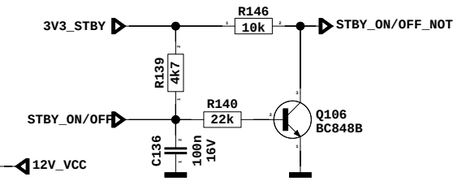
1V_VCC_CPU DC/DC (2A)



DC/DC 5
1V_VCC_CORE DC/DC (6A)



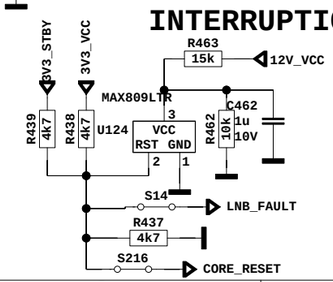
STBY On/Off Circuit



INTERRUPTION

Vout=0.6x(1+(R1/R2))

R1=20kR2=30kVout=1V



VESTEL	PROJECT NAME : 17MB185	A3
SCH NAME :POWER		T. SHT 8
DRAWN BY :<YOUR NAME HERE>		03/05/2021:16:01